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D2.1

Circuit Level Fault Models for Sub-powered CMOS Circuits for Uncorrelated and Correlated Errors

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Abstract

This deliverable presents an overview of the activities carried out within the Work Package 2 framework during the first year of the i-RISC project. These activities include circuit level analysis of sub-powered circuit components (combinational gates, memory elements, and interconnects) in deep submicron technologies, fault modeling for uncorrelated errors, as well as gate level fault injection for probabilistic fault models. We have demonstrated the fault probabilistic nature in CMOS circuits operating at sub- and near-threshold regimes. Furthermore, we have emphasized the correct output probability value dependence on circuits' inputs combination, i.e. the data dependency nature of probabilistic faults in sub-powered CMOS circuits. The results of this first phase have been further expanded into three directions: a) Probabilistic Hardware Description Language based simulated fault injection for gate level net-lists; b) Inverse Gaussian distribution delay model for sub-powered CMOS logic gates, suitable for developing fast reliability evaluation methods; and c) Markov chains based symbolic reliability analysis methodology.

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Abbreviations

CDF	Cumulative Distribution Function
CMOS	Complementary Metal Oxide Semiconductor
CSeA	Carry Select Adder
DTA	Dynamic Timing Analysis
ECC	Error Correcting Code
FPGA	Field Programmable Gate Array
HDL	Hardware Description Language
IG	Inverse Gaussian
MCSTA	Monte Carlo Static Timing Analysis
PDF	Probability Density Function
PVT	Process Voltage Temperature
RCA	Ripple Carry Adder
RTL	Register Transfer Level
SFI	Simulated Fault Injection
SSTA	Statistical Static Timing Analysis
TK	Taylor Kuznetsov
TLM	Transaction Level Modeling
TMR	Triple Modular Redundancy
WP	Work Package

1. Executive Summary

Work Package (WP) 2 aims at developing probabilistic error models for sub-powered CMOS circuits, to be utilized for fault tolerant circuit and architecture design, as well as energy characterization techniques. We pursue a hierarchical approach by proposing specific fault modeling methodologies at different abstraction layers in order to suit the i-RISC project overall goals. These include:

- Symbolic analytical methods for Error Correction Code (ECC) analysis to be utilized in WP 3 and WP 4.
- Analytical methods for fast reliability evaluation targeting the logical synthesis in WP 5.
- Simulated fault injection methodologies at different abstraction layers, e.g., gate level, Register Transfer Level (RTL), Transaction Level Modeling (TLM), as well as FPGA emulation methods for fault tolerant circuit designs evaluation to support WP 6 demonstrations activities.

WP 2 has five tasks but only 4 of them have been initiated during the first year of the project:

- T2.1 - SPICE analysis of sub-powered CMOS circuits in deep sub-micron technologies;
- T2.2 - Accurate fault models for uncorrelated errors;
- T2.3 - Accurate fault models for correlated errors;
- T2.4 - Development of simulated fault injection methodology at higher abstraction levels.

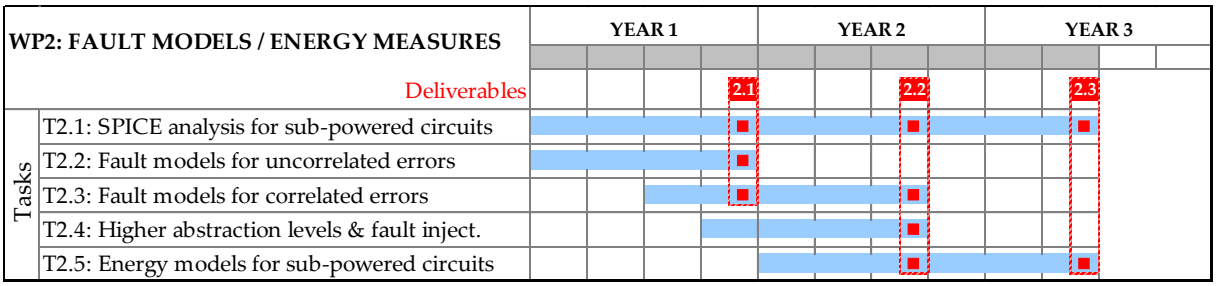


Figure 1-1: WP 2 Gantt Diagram.

T2.1 is WP 2's backbone and aims at capturing the probabilistic behavior of CMOS circuits operating at sub- and near-threshold power supply voltages and at determining the dependence of correct operation probability on external factors (e.g., power supply value, temperature), delay constraints, and input data values. T2.2 and T2.3 aim at providing analytical and symbolic methods for uncorrelated and correlated error modeling, respectively. T2.4 targets reliability assessment strategies appropriate for circuit descriptions at different abstraction layers.

WP 2 is a key project component, which strongly interacts with the other technical work-packages. As it has been specified in the first paragraph, WP2 provides assumptions and reliability assessment methods for: (i) fault tolerant code research in WP 3 and WP 4, (ii) synthesis algorithms and methodologies in WP 5, and (iii) demonstration activities in WP 6.

In this deliverable, we address the probabilistic behavior of CMOS circuits operating at sub- and near-threshold supply voltage values, as well as the analytical and gate level modeling of probabilistic faults.

The first major contribution is the introduction of delay dependent probabilistic fault models for CMOS circuits operating at very low power supply voltage values, based on a Dynamic Timing Analysis (DTA) of circuits operating at these regimes. Our SPICE simulations indicate that the main cause for probabilistic behavior for sub- and near-threshold operated circuits is their inability to deterministically complete the switching process as reaction to input transitions, given a nominal delay constraint. The probabilistic behavior is demonstrated by the wide range of switching delay values exhibited by the same gate in the presence of Process, Voltage, and Temperature (PVT) variations. Furthermore, the simulations indicate a strong dependence between gate input values and the probability of correct switching. Thus, from a logic/gate level point of view the fault models are data dependent, i.e., different correct output probabilities are obtained for different input switching combinations. We observed the strong correlation between the input values and the probability of output correctness for combinational circuits, sequential circuits, and interconnects. This represents a novel approach towards probabilistic fault modeling, as to the best of our knowledge, previous works concerning probabilistic circuits rely on a simplistic gate output probabilistic model: the logic gate has the correct output with a given probability (it does not take into account the data dependence). Therefore, the proposed models capture in a more accurate way the probabilistic behavior of sub-powered circuit. Furthermore, we also demonstrate that the probabilities for a correct output are dependent on external factors (e.g. voltage, temperature), delay constraints, and input data values.

The other contributions presented in this deliverable build upon the data/delay dependent nature of the probabilistic fault models and include:

- Gate level simulated fault injection for probabilistic circuits,
- Inverse Gaussian distribution based delay model,
- Symbolic analysis based on Markov chains.

The gate level simulated fault injection has been developed in order to address the reliability assessment of logic circuits represented by gate-level netlists. We extend existing Hardware Description Languages (HDL) based Simulated Fault Injection (SFI) frameworks and methodologies, in order to accommodate data dependent probabilistic errors. For combinational circuits we use a mutant based approach for fault injection. The main features of the proposed SFI methodology are: high flexibility (the probabilities of each gate can be mutated according to its own set of voltage, delay, and temperature parameters) and the ability to support different accuracy gate-level fault models. The proposed gate level SFI is targeted on the reliability estimation of gate-level net-lists generated during the logic synthesis process. Furthermore, we aim at extending the SFI for higher abstraction HDL descriptions.

The third contribution is the development of an Inverse Gaussian (IG) distribution based delay model for sub-powered CMOS circuits. When compared with state of the art approaches relaying on normal Gaussian distribution, our proposal exhibits a very accurate fitting for logic gates operating at both conventional and at very low supply voltages. The proposed IG distribution has two advantages as follows:

- Good scalability for logic gate chains as the parameters of the distribution for chains composed of several gates can be obtained by using a linear composition.
- Good accuracy for the reliability evaluation of probabilistic CMOS circuits – using the IG distribution Cumulative Distribution Function (CDF), the evaluated correct output probability is no more that 2% away from the one derived by means of SPICE simulations.

The IG distribution delay model provides a fast and accurate method to assess the reliability of graph based representations, e.g., And-Invert graphs, of combinational circuits. Thus, this type of model will be utilized in the logic synthesis tools developed in Work Package 5.

The fourth contribution presented in this deliverable is a Markov chain based reliability analysis method, which takes into account data dependencies. The proposed methodology represents a novel approach in symbolic reliability assessment as state of the art approaches rely on simplistic gate output probabilistic error models. Markov chains have been built for output dependence error models (which takes into account only the output), and input dependence error models (which capture the most accurately the probabilistic behavior of sub-powered CMOS circuits). A variable reduction method has been developed, in order to analyze gate net-lists composed of basic logic gates. Using the proposed Markov chain based analysis, ECC performance under faulty gates can be performed.

The deliverable is organized as follows: Chapter 2 presents the data dependent probabilistic fault models for sub-powered CMOS circuits. Chapter 3 is dedicated to the gate level simulated fault injection methodology for probabilistic circuits. The Inverse Gaussian distribution delay model is presented in Chapter 4 and the data dependence Markov chain symbolic analysis methodology is detailed in Chapter 5.

2. Probabilistic Fault Models in Sub and Near Threshold CMOS Circuits

Abstract: In this chapter, we introduce delay dependent probabilistic fault models for sub and near threshold CMOS circuits. Our SPICE Monte-Carlo simulations suggest that the main cause of the probabilistic behavior in sub-powered circuits is their inability to switch within a given delay constraint. Furthermore, the performed SPICE simulations indicated a strong dependence between the circuit inputs and the probability of correct switching. For combinational and memory circuits, this dependence can be explained by the different current loads which charge/discharge the load capacitances for different input combinations. For interconnects, capacitive and inductive influences are the main causes for this type of dependence Furthermore, we have demonstrated that glitches have a marginal effect on the overall reliability in sub-powered circuits. This is due to the very high latency that characterize sub and near threshold CMOS circuits; thus, glitch propagation for these supply voltage levels is highly unlikely.

Publications: J. Chen, S. Grandhi, C. Spagnol, A. Amaricai, S. Cotofana, and E. Popovici, "Linear Compositional Delay Model for Combinational Circuits Timing Analysis in Sub-Powered Systems" Submitted to ACM Great Lakes Symposium on VLSI (GLSVLSI), 2014.

A. Amaricai, S. Nimara, O. Boncalo, J. Chen, and E. Popovici, "Probabilistic Gate Level Fault Modeling for Near and Sub-Threshold CMOS Circuits", Submitted to European Test Symposium, 2014.

S. Nimara, A. Amaricai, and M. Popa, "Analysis of Transient Error Propagation in Sub-Powered CMOS Circuits" Accepted at 29th Int. Conf. on Microelectronics, Belgrade, May 2014

2.1. Previous Work

Probabilistic fault models for sub-powered CMOS circuits have been proposed in **[Bahar03] [Palem05] [Wang06]**. However, these models assume a very simplistic scenario, i.e., there is a certain probability that the gate output assumes an incorrect value, mostly due to thermal noise **[Karnik04][Bhanu10] [Li07]**.

Our approach in modeling probabilistic faults takes into account the large variation of the delay properties for sub-powered CMOS circuits. One major factor contributing to these is represented by the process variation characteristic to deep sub-micron technologies **[Rithe10]**. The impact of process variation is further augmented by the down scaling of the power supply voltage (Vdd) to regions where Vdd is approximately equal to transistor's threshold voltage (near-threshold) or below transistor's threshold voltage (sub-threshold) **[Agarwal02] [Hwang11]**. Other factors contributing to the undefined delay properties of CMOS circuits are the variations (noises) in the power supply and ground lines and the temperature. Due to large variation in delay associated to sub-powered CMOS gates, it is expected that the main cause for probabilistic behavior is their inability to switch correctly within a given delay. Furthermore, due to unbalanced charging/discharging paths for different input switch combinations, the probabilities for correct switching are expected to be data dependent.

2.2. Probabilistic Fault Models for Combinational Circuits

Two types of analysis were performed to model the probabilistic fault models in combinational circuits :

1. Study the delay dependent logic gate switching for sub and near threshold operating regimes for different Process, Voltage, and Temperature (PVT) conditions.
2. Transient fault propagation at very low Vdd.

HSPICE Monte-Carlo simulations have been performed for NOT, NAND, AND, Majority Voters, and XOR gates, in 45 nm CMOS technology. The considered Vdds are 0.25 V, 0.3 V, and 0.35 V. The selected temperatures are 25ºC, 50ºC, and 75ºC. The threshold voltages of the MOS transistor SPICE models are -0.302 V for the pMOS and 0.322 V for the nMOS. Hence, our analysis covers both the sub-threshold and near-threshold operation regions. The Monte-Carlo simulations consisted of 10.000 runs for each supply Vdd and temperature. Both Vdd and process variations have been considered. For supply voltage variations, a Gaussian distribution with a 0.05 V deviation has been considered. Whereas, for process variations, two sets of parameters have been considered: threshold voltage and oxide thickness. For threshold voltage a Gaussian distribution with 0.05 V deviation has been used, while for oxide thickness Gaussian distribution with 10% deviation has been employed. Following state of the art procedures **[Sutherland99]** each evaluated gate drives *4* identical gates as output loads. For the inputs, the rise and fall times are 0.1 ns, while the gate delay has been measured as the time gap between the moment when the input is crossing half of the Vdd and the moment when the output crosses Vdd/2 in reaction to the input change.

The dependence of correct switching probability, for Inverter and 2-input NAND, on the output sampling moment (i.e., the allowed propagation delay), is depicted in Figures 2-1, 2-2, and 2-3.

Figure 2-1-a presents the dependence of correct switching probability (on the *Y* axis) for the 0-1 output switching when the allowed propagation delay (on the *X* axis) is ranging from 0.1 ns to 5 ns. Figure 2-1-b represents a magnifying glass for the 2-5 ns region of the allowed propagation delay. Figure 2-2-a and 2-2-b (magnifying glass of 2-2-a) presents the dependence of correct switching probability (on the *Y* axis) for the 1-0 output switching on the allowed propagation delay (on the *X* axis). These two figures indicate:

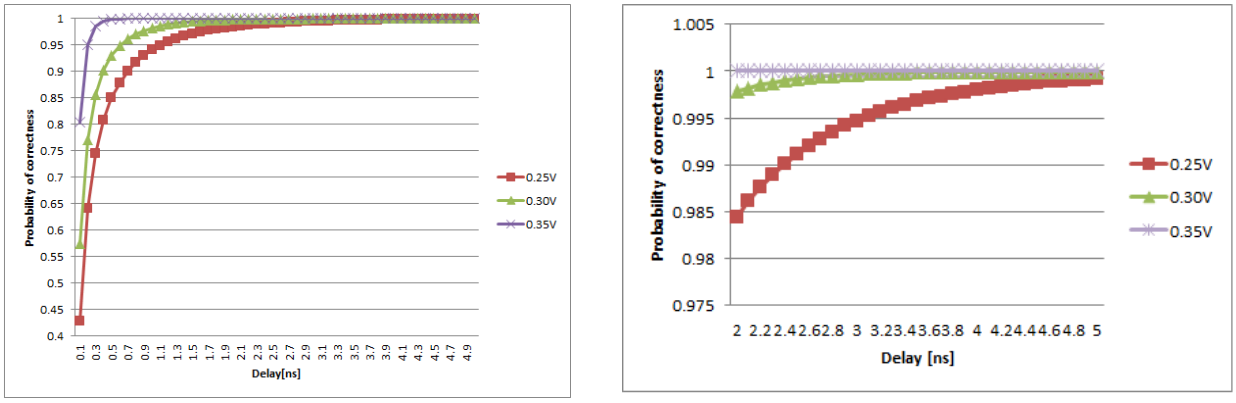
1. The increase in the allowed gate delay leads to an increase in correct switching probability; for very large gate delay constraints (e.g. 3 ns for Vdd = 0.35V) the gate switches correctly with a probability of 1
2. A higher Vdd leads to a higher correct switching probability; this is explained by the higher performance (lower gate delay) associated with higher power supply voltages.
3. Different probabilities are obtained for the two switching scenarios; the correct switching probability for 1-0 output switch is higher with respect to the one for 0-1 switch; this is due to the different driving strength of the pMOS and nMOS transistors in the inverter;

Figure 2-3 presents the dependence of correct switching probability on the allowed propagation delay for a 2-input NAND when the inputs switch from 00-11 (a), 01-11 (b), 11-00 (c) or 11-01 (d). The first two observations presented above for the inverter apply also for the 2-input NAND gate. Furthermore, figure 3-3 indicates the different correct switching probabilities for the 4 input transitions. The lowest probability is obtained for the 11-01 input transition; this is due to the low

driving strength of a single pMOS transistor. The highest probability is obtained for the 11-00 input transition; in this case the charging current load is given by the 2 parallel pMOS transistors.

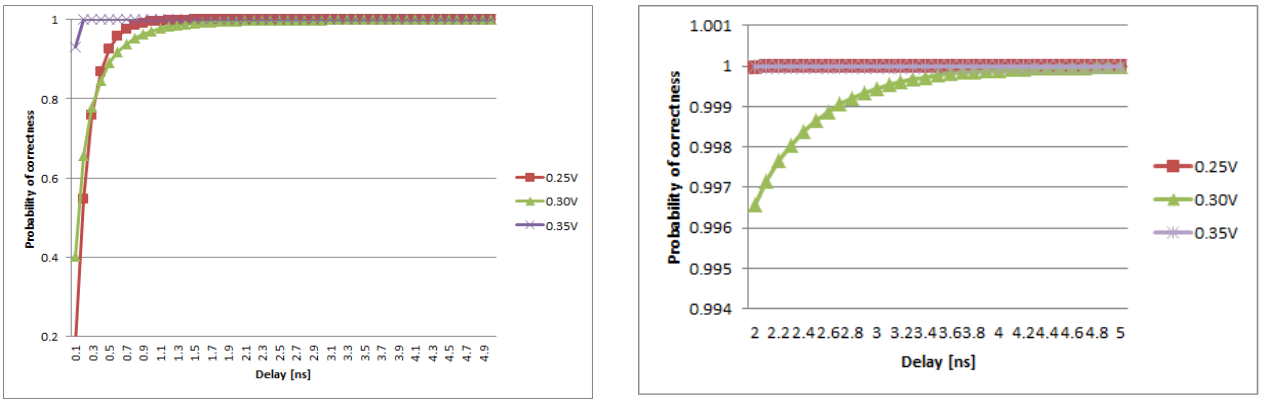
We note that for our study, we made a number of assumptions, e.g., input transitions from 11 to 10 and from 11 to 01 are similar, neglect the skew at input signals. Those helped us to simplify the analysis without major impact on the probabilistic nature of switching for sub-powered CMOS logic gates behavior.

Results which indicate the three observations drawn from Inverter and 2-input NAND gate (the dependence between the correct switch probability and the allowed gate delay, the dependence between the correct switch probability and the Vdd, and the dependence between switch probability and the input transition) have also been obtained for 2-input AND, 3-input XOR and Majority gate.



a) b)

Figure 2-1: Output Correctness vs Delay (Inverter @ 25ºC for 0-1 Output Switching).



a) b)

Figure 2-2: Output Correctness vs Delay (Inverter @ 25ºC for 1-0 Output Switching).

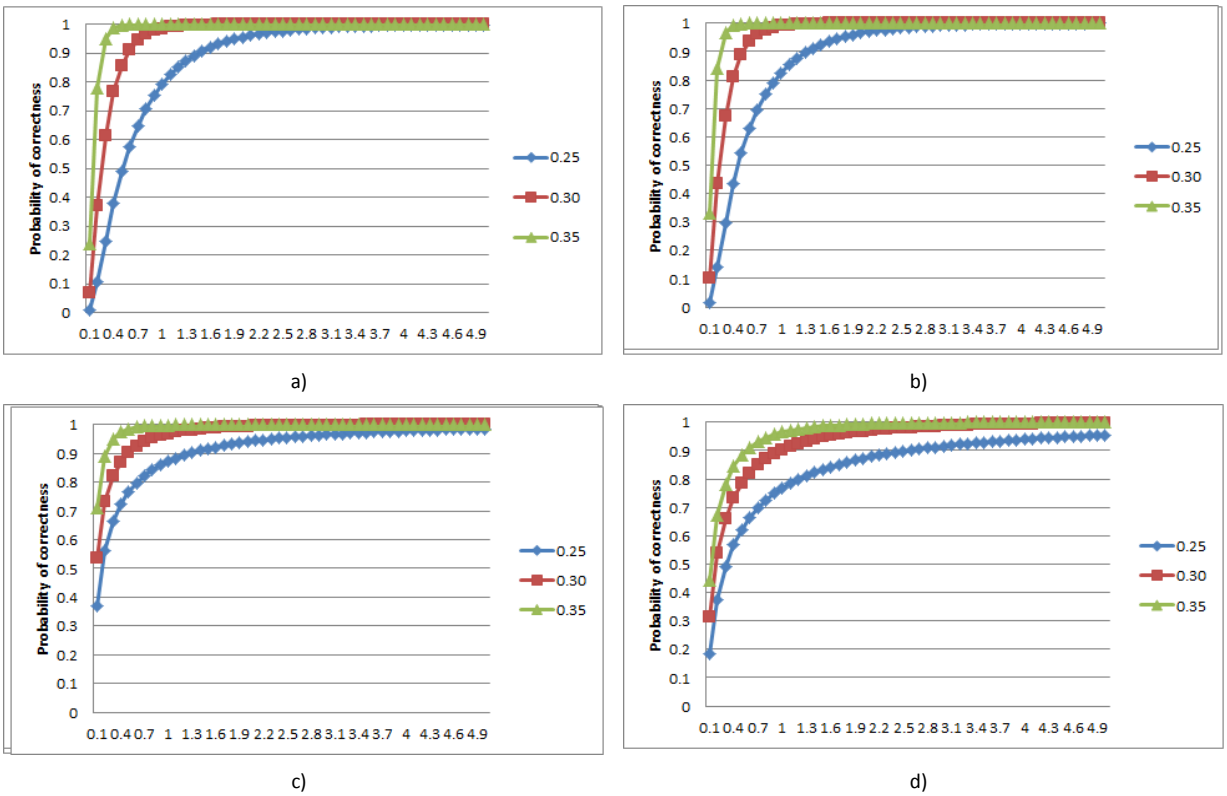
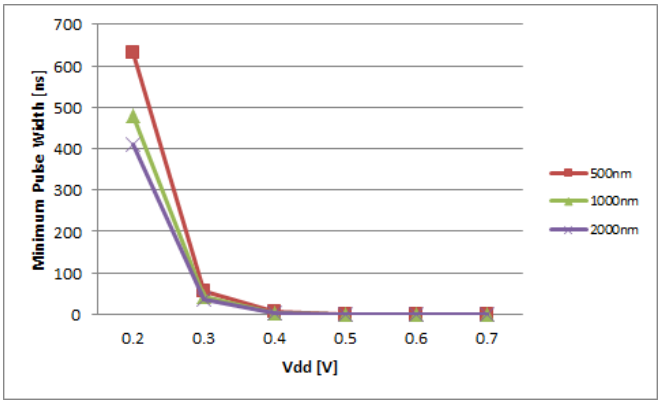
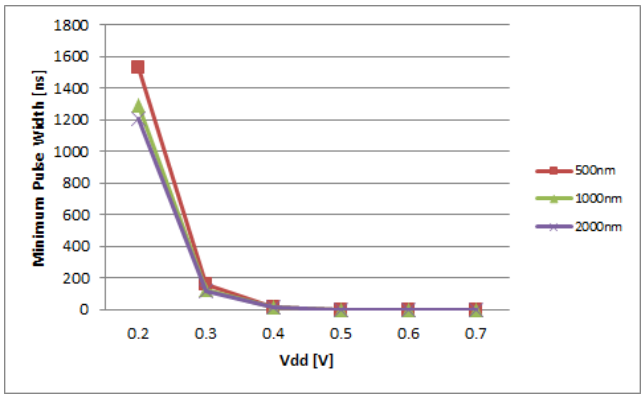


Figure 2-3: Output Correctness vs Delay for 2-input NAND @ 25ºC for Different Input Transitions: a) 00 to 11, b) 01 or 10 to 11, c) 11 to 00, and d) 11 to 01 or 10.

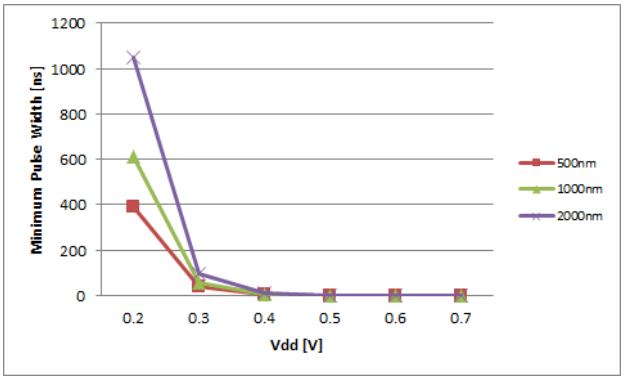
The second type of analysis has investigated the propagation of glitches in circuits for sub and near threshold supply voltages. The goal of our analysis is to determine the minimum glitch width/duration present at gate's input which ensures an erroneous gate output. Undesired glitches are the result of single event transients produced by factors, e.g., radiation (single particle hit), IR drop **[Zivanov10]**. Figures 2-4 and 2-5 present the dependence between the supply voltage and the minimum glitch duration, which ensures propagation through inverters. The simulations have been performed in SPICE for 45 nm Predictive Technology Model (PTM) transistor models. For the inverter the following ratios between the pMOS and nMOS transistor widths have been considered: 1, 2, and 4. For the NAND gates the following transistor ratios widths have been considered: 0.5, 1 and 2.



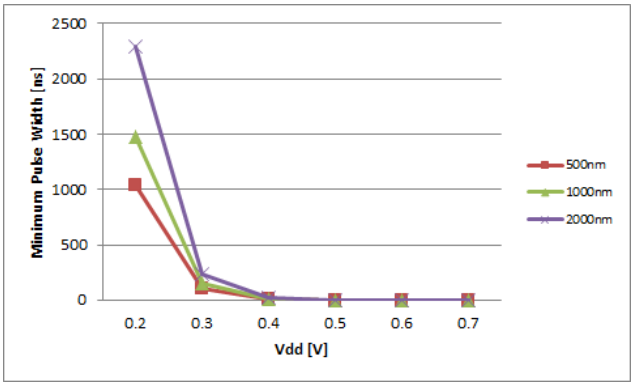


b)

Figure 2-4: Minimum Propagable 1-0-1 Glitch Width a) Inverter; b) 2-Inverter Chain.



a)



b)

Figure 2-5: Minimum Propagable 0-1-0 Glitch Width a) Inverter; b) 2-Inverter Chain.

The results depicted in the figures indicate that electrical masking effects (attenuation or complete masking due to low duration of the glitch compared to the gate delay) dominate at sub and near threshold supply voltages. For Vdd 0.3 V the minimum glitch width which ensures propagation through a single inverter is 36 ns, while the minimum width which ensures propagation through 2 inverter gates is 117 ns. Thus, although the logic gates may be more prone to single event transients at very low supply voltages (more glitches may appear at such low levels of Vdd), they do not impact in a significant way the overall reliability of the circuit due to their limited propagation through a logic circuit. Furthermore, for higher pMOS/nMOS widths ratios, a 1-0-1 glitch at the inverter's input is more likely to propagate.

The two types of simulations have clearly indicated that the most important reliability issue in the sub and near threshold regime is the logic gate inability to deterministically accomplish the switching process within the a given period of time. Furthermore, we observe that the logic gate output value correctness probability is data dependent as different probabilities are obtained for different input value transitions.

2.3. Probabilistic Fault Models for Sequential Circuits

Delay dependent reliability evaluation has been performed for the NAND based D flip-flop. The results for 0.3 V supply voltage are presented in Fig 2-6. For the considered D flip-flop, the delay has been measured as the time gap between clock edge cross half of the supply voltage and output cross half of Vdd. As depicted, one can observe in Fig. 2-6 that the output correctness probability is dependent on the type of switching (charging or discharging the D flip-flop output).

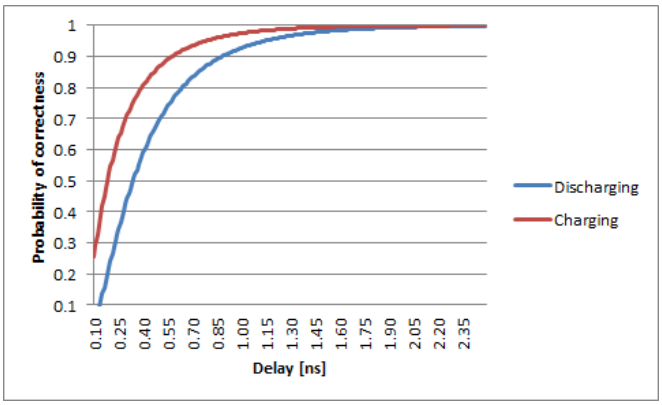


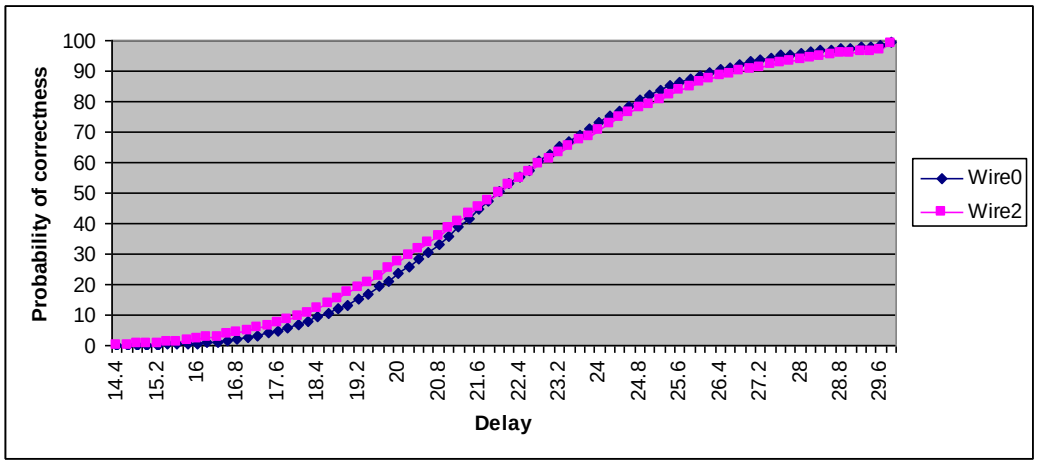
Figure 2-6: Output Correctness vs Delay (D flip-flop @ Vdd = 0.3V).

The probabilistic nature of fault models for this type of memory element is similar with the ones obtained for combinational circuits. As obtained in logic gates, the probability of D flip-flop correct switching is data dependent, while delay constraints represent an important factor in the overall reliability of the circuit.

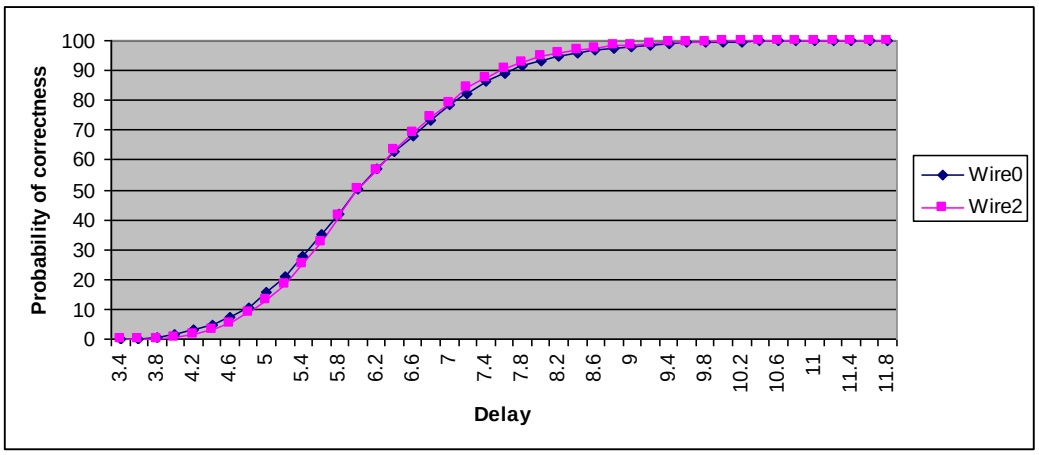
2.4. Probabilistic Fault Models for Interconnects

Monte Carlo SPICE simulations have been performed for interconnect consisting of 3 wires driven by 3 inverter gates. A PTM resistance (R), inductance (L), capacitor (C) model for a local interconnect has been used, while the drivers have been implemented using 45 nm PTM transistor models **[Zhao06][PTM]**. The simulated wires have the following dimensions: 50 µm length, 70 nm spacing between 2 wires, a 70 nm width, 150 nm thickness, and 150 nm height from ground plates. The considered supply voltages are 0.25V, 0.3 V, and 0.35 V. We have simulated interconnect structures in the context of voltage and process parameter variations. The process variations were reflected in variation of the interconnect RLC parameters. These process variations have a wide range of causes: dishing, erosion, metal defects (such as holes in the metal layers), via and contact size variations, oxide loss, dielectric constant variation, etc. **[Boning99]**. The process variations have been applied only to metal wires and not for the wire drivers. Although we have simulated local interconnects with

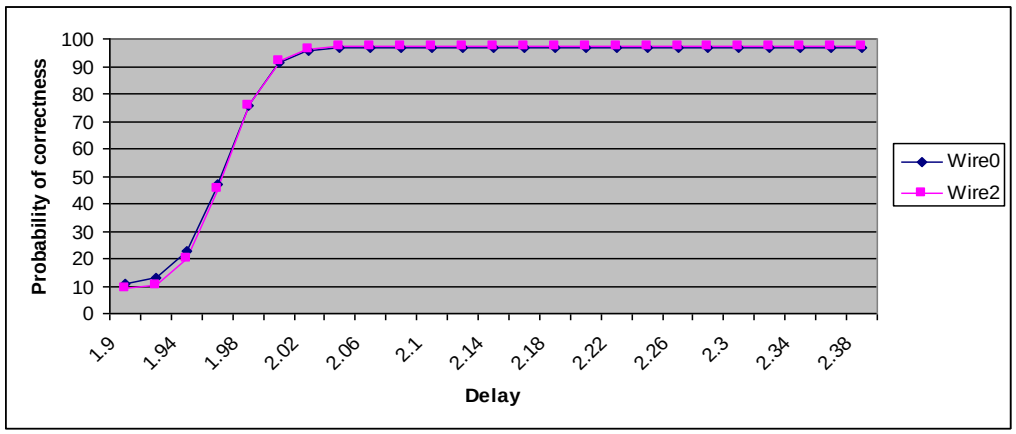
simple driver buffers, the same methodology can be applied for intermediate and global interconnect with dedicated repeater buffers. We have performed Monte Carlo consisting of 5000 simulations for all input transition combinations (35 input transition combinations for 3 wires).



a)

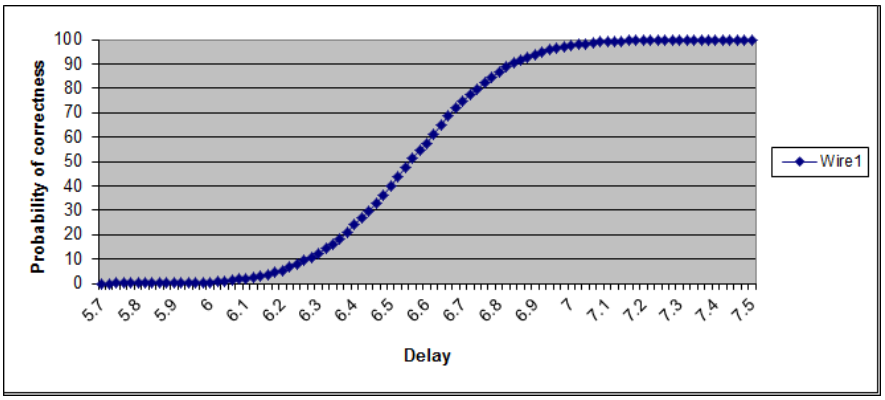


b)

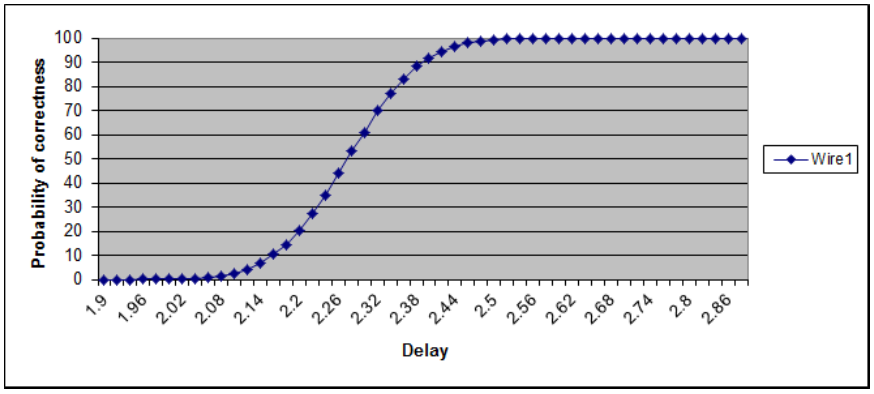


c)

Figure 2-7: Correct 111 – 010 Switching Probability: 3-wire Interconnects
a) Vdd=0.25V, b) Vdd=0.3 V, and c) Vdd=0.35V.



a)



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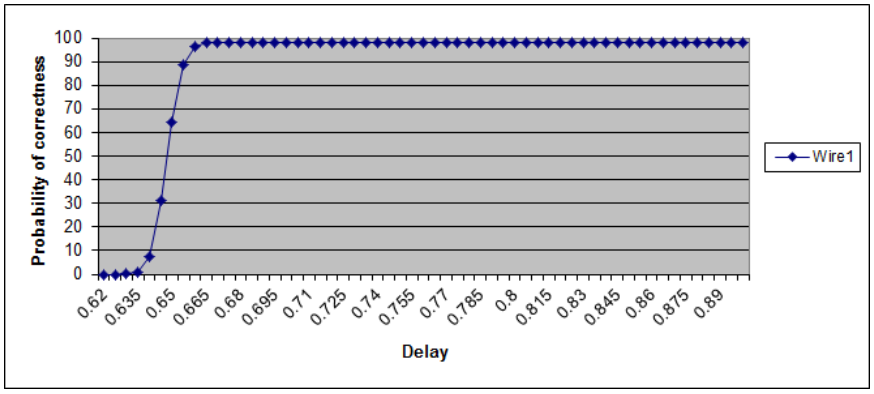


c)

Figure 2-8: Correct 000 – 001 Switching Probability: 3-wire Interconnects
a) Vdd=0.25V, b) Vdd=0.3 V, and c) Vdd=0.35V.

Figures 2-7 and 2-8 depict the results for 2 input configurations for the three considered supply voltages. The simulations indicate the following:

a. Higher allowed delay leads to higher correct switching probability.

b. Higher Vdd leads to higher correct switching probability for the same delay constrained.

c. A stronger dependence between the inputs values and the probability of correct switching for a given delay constraint with respect to logic circuits. For example, from the above figures we observe the large delays differences between the switching times from 111-010 and from 000 – 001.

Regarding c., this is mainly determined by the influence of the capacitive and inductive crosstalk on the switching process.

2.5. Conclusion

In this chapter we presented circuit-level analysis results for CMOS combinational circuits, memory elements, and interconnects operating at sub and near threshold supply voltages. The overall conclusions we can draw from our experiments can be stated as follows:

1. The main cause of the probabilistic nature of fault models in CMOS circuits operating at very low supply voltages is the inability of the circuit to deterministically accomplish the switching process within a given delay constraint. Furthermore, gates present an increasing, with the Vdd down scaling, wide range of delays for the same input combination under PVT variations.
2. The probability of correct switching for a given circuit is data dependent; for combinational and sequential circuits, this is due to different current loads passing through the NMOS/PMOS stages which charge/discharge the load capacitance. For interconnects, the main cause is represented by the wire capacitive and inductive cross-coupling.
3. Transient faults have marginal effect on the overall circuit reliability mainly due to electrical masking effects, which are present at very low supply voltages, which limits their propagation within a circuit. Thus, we can conclude that transients have a marginal effect on the overall reliability of sub-powered CMOS circuits.

The circuit level analysis will be extended in three main directions:

1. Developing probability density functions (PDF) for combinational and sequential circuits – these mathematical models will be used in reliability estimation of gate net-lists obtained in the synthesis process (WP5); a strong requirement for logic synthesis of reliable circuits is represent by the development of a reliability metric estimator, based on the reliability function (expressed as a static probability or as a PDF) of the basic components
2. Developing gate-level and RTL simulated fault injection methodology – the simulated fault injection will be used for estimating reliability of gate-level and/or RTL proof-of concepts designs developed in WP6.
3. Developing symbolic fault analysis – these type of analysis allows early estimation of ECC performance for logic, memories and interconnects (WP3 and WP4)

For each of the three directions, work has been initiated in this first year of the project and will be detailed in the following chapters.

3. Gate Level Simulated Fault Injection for Probabilistic Sub-Powered CMOS Combinational Circuits

Abstract In this chapter, a methodology for the simulated fault injection of probabilistic errors in gate level netlists for combinational circuits is presented. Based on the results presented in Chapter 2, we have derived four probabilistic fault models, with different accuracies. For gate level descriptions, we have employed a mutant based approach. The proposed approach introduces a 2x to 5x simulation overhead with respect to the "gold" circuit simulation and requires 3 orders of magnitude less simulation time with respect to SPICE simulation.

Publications: Part of this work has been submitted to:

A. Amaricai, S. Nimara, O. Boncalo, J. Chen, and E. Popovici, "Probabilistic Gate Level Fault Modeling for Near and Sub-Threshold CMOS Circuits", Submitted to European Test Symposium, 2014.

3.1. Simulated Fault Injection

Hardware description languages (HDL) based simulated fault represents a powerful method to analyze the circuit behavior in the presence of a wide range of faults **[Jenn94] [Gil08] [Seward03] [Sheng08]**. SFI can be applied as soon as the corresponding abstraction layer description is available in the design phase. The key ingredient for good results from the fault injection process is an appropriate fault model. This techniques have been used to study the effect of permanent faults **[Jenn94] [Gil08]** and of transient faults **[Gil08] [Seward03] [Sheng08] [Mansour12]** that result in single event upsets and single event transients for, e.g., Leon3 microprocessor **[Mansour12]**, commercial microcontrollers **[Gil08]**. Fault injection techniques have been classified in two main categories **[Jenn94]**: approaches that do not require code modification (i.e., simulator commands and scripts **[Sheng08]**) and those that require modifications of the HDL code (mutants and saboteurs **[Jenn94] [Gil08]**). The techniques based on code intervention either alter the characteristics of the signals from a structural description (*saboteurs*), or replace correct component architecture with a faulty one (i.e., *mutants*). Although techniques based on simulator commands or scripts do not require code intervention, they are dependent on the simulator environment capabilities. Furthermore, unless a tool such as the one presented in **[Sheng08]** is available, the applicability of this technique for large circuits is cumbersome. The techniques based on HDL code modification require significant design rework, however, their fault modelling capability is high. Typically an SFI campaign consists of three phases **[Jenn94] [Gil08]**: the set-up phase (select fault models, fault locations, number of runs, do the required changes on the simulation model and or prepare simulation scripts), the simulation phase (when the actual simulation takes place), and the data processing/analysis phase (deriving the reliability metrics).

For gate level descriptions, we have implemented mutant based SFI, as they present very good component (in our case logic gates) based fault modeling capability (with respect to saboteur which presents good signal based fault modeling capability).

3.2. Gate Level Fault Models

The simulation results have shown the probabilistic nature of the fault models in sub and near threshold regimes. The following four fault models have been derived for gate level simulations:

1. Gate Output Probabilistic model (GOP) – For this model, the gate has the correct output with a given probability. The faulty output may appear due to two factors: a random bit-flip of the output (similar to a single event transient) or the inability of the gate to complete the switching within a certain delay constraint. As discussed in Section 3.1, undesired bit-flips may have negligible effects on the overall circuit output, due to their ability to propagate through the circuit.
2. Gate Output Switching probabilistic model (GOS) – For this model, probabilistic behavior occurs only when the gate switches. The probability of correct switching is dependent on the external factors, such supply voltage, temperature, etc.
3. Gate Output Switching Type probabilistic model (GOST) – Compared to the previous model, different probabilities for output charging and discharging are considered. The different probabilities for each type of switching are a consequence of different drive strength of gate nMOS and pMOS stages. For balanced nMOS and pMOS stages, this fault model is equivalent to GOS.
4. Gate Input Switching Probabilistic model (GISP) – For this model, different probabilities are assumed for each of the input switching combination. It is justified by the fact that each input determines the turn-on/turn-off of a pair of nMOS/pMOS gate transistors. This model captures in the most accurate way the probabilistic behavior described in Chapter 2.

For these four models, the probabilities are expressed as a constant given for a considered supply voltage, temperature, and delay constraint.

3.3. Simulated Fault Injection Methodology

We have developed an SFI methodology based on mutants for reliability analysis. The SFI techniques have been implemented in Verilog HDL, however, their extension to VHDL can be easily performed. We decided to utilize Verilog for a better interaction with WP 5 as the modified ABC synthesis tool outputs Verilog gate netlists. Figure 3-1 depicts the SFI methodology, which consists of two phases: (i) setup phase and (ii) simulation and result analysis phase.

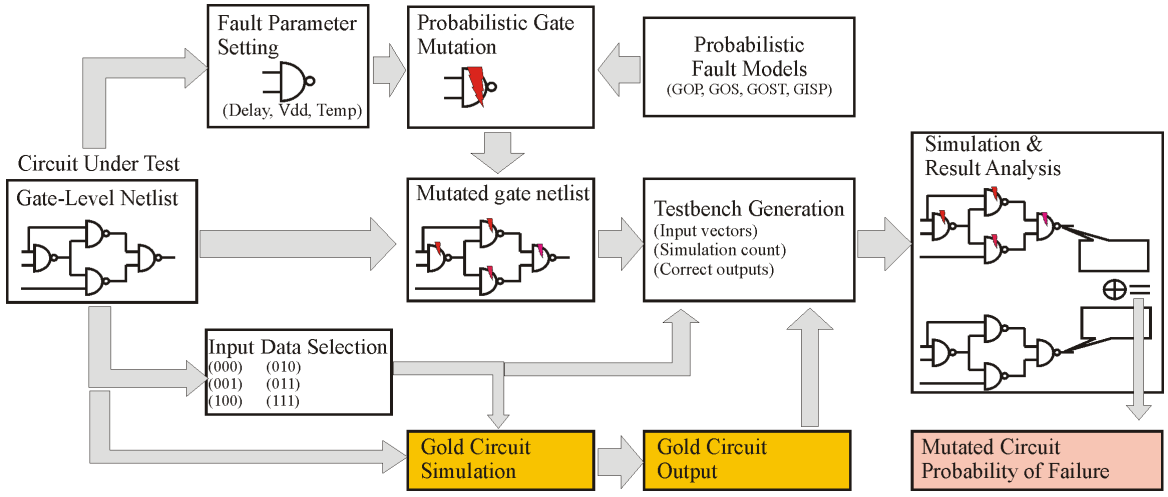


Figure 3-1: Simulated Fault Injection Process for Probabilistic Error Analysis.

The setup phase comprises of the following steps:

1. Fault parameter settings – The three parameters (gate delay, power supply voltage (Vdd), and temperature) are set for each gate. Note that each gate can have its own independent set of parameters, thus, we can simulate a wide range of scenarios: unbalanced delay paths, multiple voltage islands, regions of the circuit with different heating.

2. Probabilistic gate mutation – Based on the gate fault parameters and the fault model, the corresponding mutation is selected for each gate and the mutated circuit netlist is created.

3. Input data selection – Because GOS, GOST, and GISP fault models are data dependent, circuit input data represents a very important aspect in the reliability analysis.

4. Gold circuit simulation – The correct outputs are required for determining the reliability parameters. Therefore, simulation of the gold circuit with the selected input data has to be performed.

5. Testbench generation – Input data, correct output, and the number of simulation are considered when developing the testbench module/entity. This testbench is meant to provide both simulation control and result analysis.

The second phase consists of the actual simulation and result analysis. Due to probabilistic nature of the fault models, a large number of simulations are required. Result analysis procedures are included in the devised testbench, therefore, this stage is performed almost simultaneously with the simulation.

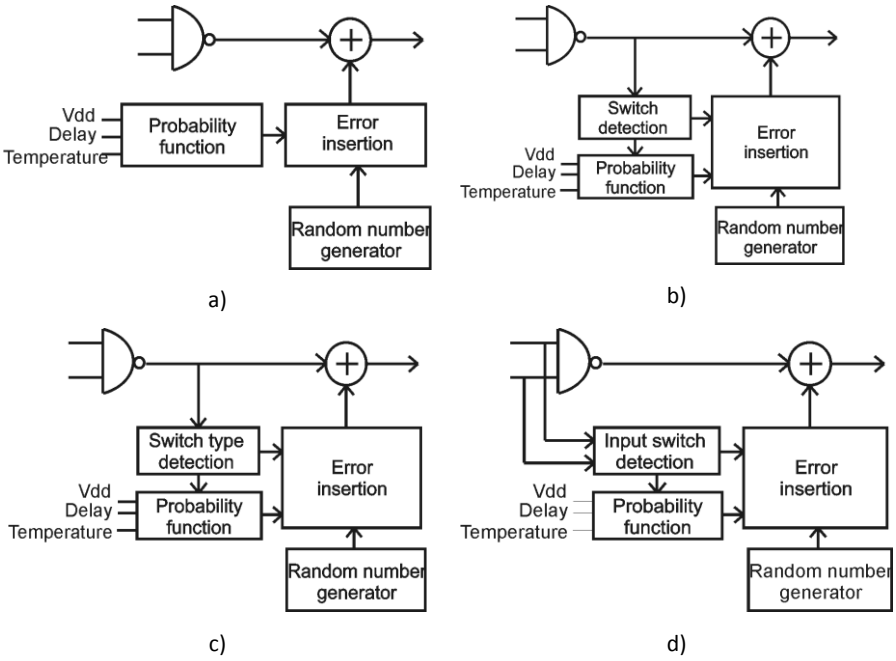


Figure 3-2: NAND Gate Mutated Architectures.

The mutant was the technique of choice for implementing probabilistic fault injection. For each of the four fault models, a mutant architecture has been designed. Their construction is depicted in Figure 3-2. All the mutants include a random number generator and a probability function (which computes the probability according to the desired Vdd, delay constraint and temperature). The Vdd,

delay, and temperature set of parameters can be tuned for each mutated component. This feature allows great flexibility for the proposed SFI. Thus, we can simulate different circuit configurations, such as: circuits with unbalanced delay paths, circuits with multiple voltage islands, circuits with different heating regions, etc. According to the fault model, output or input switch detection is implemented.

```
module gate_different_switching_characteristics

  switch_type = detectOutputSwitchingType();
  if (switch_type == 01) then
      // generate random number
      rand_nr1 = randomNumberGenerator();
      // calculate the gate failure probability
      PTF1 = errorModel3(vdd, delay, temp);
      // failure condition
      fail = generate_probabilistic_failure(rand_nr1, PTF1);
      output = fail ? (incorrect_op) : (correct_op);

  if (switch_type == 10) then
      rand_nr2 = randomNumberGenerator();
      PTF2 = errorModel3(vdd, delay, temp);
      fail = generate_probabilistic_failure(rand_nr2, PTF2);
      output = fail ? (incorrect_op) : (correct_op);
```

Figure 3-3: Pseudo-code Associated to GOST Fault Models.

The pseudo-code associated to the mutant modules which implement GOST fault models are depicted in Figure 3-3. For this model, the output switching type detection is performed; for each switching type, a different probability function is used.

3.4. Simulation Results

We have simulated 6-bit adders in three configurations: Ripple Carry Adders (RCA), Carry Select Adders (CSeA), and fault tolerant Triple Modular Redundant (TMR) RCAs. We have computed the probability of correctness for each bit and for entire sum. 6-bit adders have been chosen because they important components in variable node units and check node units of LDPC decoders. The adders have been implemented using only 2-input NAND gates. In this case, the number of gates is consistently higher with the XOR/Majority Logic implementation. The main goal of these campaigns is to showcase the flexibility of the proposed probabilistic mutant based approach and to analyze the simulation overhead required in the reliability analysis based on fault injection. The simulations have been performed using Modelsim 10.05 SE commercial simulator on Windows 7 OS. Each simulation campaign consist of 48 000 simulations (we have used the GOS, GOST and GISP fault models and for each fault model we have performed 16000 simulation). Results are depicted in Table 3-1 (RCA), Table 3-2 (CSeA), and Table 3-3 (TMR).

Table 3-1: 6-bit RCA Simulation Results.

Circuit	Fault Model	Delay (ns)	Vdd (V)	Sum Bits Failure Probabilities							Circuit Failure Prob.	Sim. Time (s)
				6	5	4	3	2	1	0		
6-bit RCA	GOS	1.5	0.35	1.01	2.34	3.05	2.88	2.74	1.90	1.66	10.16	1
			0.30	6.38	13.50	16.53	16.72	15.63	11.53	10.84	50.09	2
			0.25	22.63	39.07	42.90	42.28	43.79	37.58	35.80	90.16	2
	GOST	1.5	0.35	0.97	2.03	2.56	2.54	2.39	1.88	1.86	9.46	1
			0.30	5.23	13.19	14.59	15.19	14.14	10.48	12.54	49.53	1
			0.25	21.25	39.09	41.06	42.56	42.73	38.19	37.27	90.03	1
	GISP	1.5	0.35	0.99	2.94	3.25	3.44	3.31	2.51	2.60	12.96	1
			0.30	5.50	14.22	17.48	17.66	17.79	12.56	15.59	55.44	1
			0.25	20.08	39.29	41.18	43.59	43.74	41.29	39.79	90.48	1
6-bit RCA	GOS	Carry chain 1 Sum gates 1-4	0.35	3.34	7.27	7.66	6.88	5.76	3.21	3.44	20.44	1
			0.30	12.39	25.73	26.02	25.28	21.58	12.78	13.77	64.03	1
			0.25	35.61	48.42	45.68	46.68	46.16	38.21	45.53	92.41	2
	GOST	Carry chain 1 Sum gates 1-4	0.35	3.10	6.50	6.39	5.97	5.29	2.09	3.54	18.53	2
			0.30	11.26	24.14	24.21	24.16	21.49	10.78	14.91	62.16	2
			0.25	31.89	46.72	44.44	46.26	46.03	36.71	44.85	92.03	1
	GISP	Carry chain 1 Sum gates 1-4	0.35	3.11	7.73	8.41	8.26	6.76	3.06	4.75	22.73	1
			0.30	10.99	24.79	25.81	25.96	21.89	11.94	17.64	65.64	2
			0.25	33.38	46.11	45.63	46.84	47.01	39.16	46.66	92.31	1
Gold 6-bit RCA				-	-	-	-	-	-	-	-	0.5

Table 3-2: 6-bit CSeA Simulation Results.

Circuit	Fault Model	Delay (ns)	Vdd (V)	Sum Bits Failure Probabilities							Circuit Failure Prob.	Sim. Time (s)
				6	5	4	3	2	1	0		
6-bit CSeA	GOS	1.5	0.35	1.39	3.13	3.69	3.99	2.91	1.79	1.66	12.17	1
			0.30	8.73	15.84	18.90	19.04	15.01	11.24	11.03	55.59	1
			0.25	29.81	39.71	42.14	44.28	42.28	37.73	36.83	91.09	2
	GOST	1.5	0.35	1.35	2.73	3.08	3.26	2.32	1.58	1.91	11.35	1
			0.30	6.96	14.23	16.51	18.29	14.34	11.28	12.99	54.36	1
			0.25	26.28	36.64	40.93	44.69	42.66	38.75	37.21	90.64	2
	GISP	1.5	0.35	1.14	3.23	4.04	3.98	3.10	2.29	2.56	14.13	1
			0.30	6.53	15.95	20.18	21.51	17.80	13.17	15.69	59.55	1
			0.25	26.09	39.94	41.50	45.06	45.11	40.64	39.85	91.70	1
6-bit CSeA	GOS	Carry chain 1 Sum gates 1-4 Mux 1.5	0.35	1.39	3.13	3.69	3.99	2.91	1.79	1.66	12.17	2
			0.30	8.73	15.84	18.90	19.04	15.01	11.24	11.03	55.59	1
			0.25	29.81	39.71	42.14	44.28	42.28	37.73	36.83	91.09	1
	GOST	Carry chain 1 Sum gates 1-4 Mux 1.5	0.35	1.35	2.73	3.08	3.26	2.32	1.58	1.91	11.35	1
			0.30	6.96	14.23	16.51	18.29	14.34	11.28	12.99	54.36	2
			0.25	26.28	36.64	40.93	44.69	42.66	38.75	37.21	90.64	2

	GISP	Carry chain 1 Sum gates 1-4 Mux 1.5	0.35	1.14	3.23	4.04	3.98	3.10	2.29	2.56	14.13	1
			0.30	6.53	15.95	20.18	21.51	17.80	13.17	15.69	59.55	2
			0.25	26.09	39.94	41.50	45.06	45.11	40.64	39.85	91.70	1
Gold 6-bit CSeA				-	-	-	-	-	-	-	-	0.5

Table 3-3: 6-bit TMR Based RCA Simulation Results.

Circuit	Fault Model	Delay (ns)	Vdd (V)	Sum Bits Failure Probabilities							Circuit Failure Prob.	Sim. Time (s)
				6	5	4	3	2	1	0		
TMR 6-bit RCA	GOS	Carry chain 1 Sum gates 1-4 Voter 2	0.30	10.99	20.72	20.99	17.88	14.71	7.99	8.15	56.81	5
	GOST	Carry chain 1 Sum gates 1-4 Voter 2	0.30	12.46	20.33	19.84	17.83	14.46	8.33	9.87	57.09	4
	GISP	Carry chain 1 Sum gates 1-4 Voter 2	0.30	10.29	21.14	21.74	20.61	16.33	7.81	10.73	57.88	4
TMR 6-bit RCA	GOS	Carry chain 1 Sum gates 1-4 Voter 2	Adder 0.3 Voter 0.35	8.05	18.69	19.19	17.02	12.37	4.75	6.14	48.23	5
	GOST	Carry chain 1 Sum gates 1-4 Voter 2	Adder 0.3 Voter 0.35	8.83	17.53	17.71	16.21	11.95	4.83	6.11	46.39	4
	GISP	Carry chain 1 Sum gates 1-4 Voter 2	Adder 0.3 Voter 0.35	9.16	18.60	20.09	18.85	13.79	5.55	8.56	50.94	4
Gold TMR 6-bit RCA				-	-	-	-	-	-	-	-	1

In the first campaigns (first rows) in Tables 3-1 and 3-2, all the gates in the RCA and CSeA have the same delay constraints. The second campaigns in Tables 3-1 and 3-2 have considered the more realistic case when the gates have different delay constraints. Regarding the TMR (Table 3-3), two cases have been considered: all the circuit operates at the same Vdd, and the adders operate at lower Vdd, while the voter operates at higher Vdd. The former is of interest in the context of our project: the computational/logic components, data transport and data storage are expected to operate at lower Vdd for better energy consumption; the components which perform error detection and correction are expected to operate at higher Vdd for better reliability.

Regarding the results of the simulations, we observe that the CSeA configuration has better reliability with respect to the RCA. Furthermore, we observe that the TMR configuration (when all

the circuit operates at the same Vdd) does not significantly improve the reliability of the RCA for the considered gate probabilities. Both the RCA and the RCA in TMR configuration at Vdd=0.3V are more likely to give an erroneous result (the probability of erroneous output is higher than 50%).

The results indicate that in 6-bit adders (with carry-out), the most error prone bits are the most significant three bits of the sum (bits 4, 5, and 3). The most "resilient" bits are the least significant bits (bits 0 and 1) followed by the carry-out bit.

The last rows of the tables present simulation times for "gold" circuit implementation. With respect to gold circuit simulation, the proposed SFI introduces a substantial simulation time overhead (simulation time is 2-5x times longer). This is due two factors: the fault injection mechanism and the result analysis, which is also performed in the simulation. For small and medium circuits, which consist of up to several thousand gates, simulation times are negligible (maximum 5s), despite the high number of input vectors (16 000). For large and very large circuits (composed of millions of gates), the proposed method may have some limitations, which are due to: i) the high number of input vectors combinations (which increases exponentially with the number of inputs); ii) gate level simulation is time consuming for very large circuits. However, small and medium circuits comparable to the ones presented in Tables 3.1-3.3 usually compose building blocks (functional units, multiplexers, decoders, registers, etc.) present in RTL descriptions. Furthermore, gate level simulation is necessary for our goal of developing hierarchical simulation based reliability assessment.

3.5. Conclusion

We have developed a highly flexible mutant based SFI methodology for gate level netlists described combinational circuits. Our mutant techniques implement four types of probabilistic fault models. The proposed mutant based SFI is characterized by high flexibility; each gate in the circuit description can be tuned with its own probability, according to the desired temperature, Vdd, and delay constraint.

The proposed SFI introduces a 2x to 5x simulation time overhead when compared to gold circuit simulation. However, for small and medium circuits, the proposed approach has negligible simulation times (several seconds).

4. Linear Compositional Delay Model for Sub-Powered CMOS Circuits

Abstract: In this chapter, we introduce an Inverse Gaussian (IG) model, which is able to accurately capture the delay distribution for process, voltage, and temperature (PVT) variation at low power supply voltages (Vdd). For this model, linear compositionality can easily be implemented in order to propagate the mean and the shape parameters of the model, for medium and large combinational circuits. The average error of this model, when compared to Monte Carlo SPICE simulations, is less than 2% for both nominal, near, and sub threshold Vdd. Thus, this IG model provides very good accuracy, with a speedup at least 10000 times with respect to SPICE simulations.

Publications: J. Chen, S. Grandhi, C. Spagnol, A. Amaricai, S. Cotofana, and E. Popovici, "Linear Compositional Delay Model for Combinational Circuits Timing Analysis in Sub-Powered Systems", Submitted to the ACM Great Lakes Symposium on VLSI (GLSVLSI), 2014.

4.1. Previous Work

Delay variation represents one of the major issues in today's synchronous design. Usually, corner analysis has been a popular approach of dealing with delay variation. However, it has the limitation of being overly pessimistic or optimistic **[Hwang11].** Therefore, a simple yet accurate mathematical model to evaluate the propagation of nano CMOS is highly desirable.

Previous attempts, which tried to use mathematical delay models for CMOS circuits, had relied on the normal Gaussian distribution. In **[Zaynoun12]** a 2-input CMOS AND gate was evaluated by means of Spice simulations, while the threshold voltage variation, as the most dominant element of all process variations, was modeled with a normal (Gaussian) distribution. 32nm Predictive Transistor Models (PTM) under a nominal supply voltage of 0.9V were considered to build the AND gate and perform Monte Carlo simulation. Close matches were found between the measured propagation delay profile and the Gaussian Probability Density Function (PDF). Based on this assumption a propagation delay estimation algorithm was presented. However, the choice of approximating the delay PDF with a normal distribution was based on the fitting of only two Monte Carlo simulations. Being just a fitting procedure, no theoretical explanation was possible to support the conclusion. Furthermore, these models have considered only nominal Vdd. Thus, the proposed delay model will try also to address also the near and sub-threshold regions of operations.

4.2. Inverse Gaussian Approximation

In our approach we have chosen an IG distribution to model the delay distribution for nominal, near, and sub threshold CMOS circuits operation regimes. The selection of this type of distribution has also an intuitive reason: it accurately describes the particles motion when a drift is applied. For semiconductor devices, the drift is associated to the voltage differences between transistors' terminals, while particles are represented by charge carriers. The IG distribution PDF is given by Eq. 5-1, while its main parameters are μ (the mean parameter) and λ (the shape parameter). The distribution support is $[0,\infty]$ and it can be symmetric or asymmetric around μ.

$$f(x,\mu,\lambda)=\sqrt{\lambda/2\pi x^3}*e^{\frac{-\lambda(x-\mu)^2}{2\mu^2 x}};x>0 \qquad (4\text{-}1)$$

Figure 4-1 presents the fitting of the IG distribution and of the normal Gaussian distribution for a 2-input AND gate supplied at 0.3 V. The bars represent the densities obtained in SPICE simulation. The voltage and process variations have followed a normal distribution. Figure 4-2 depicts the fitting of the IG and normal distributions on chains of 3 and 5 2-input AND gates at 0.9 V nominal supply voltage.

In Figure 5-3 the fitting of the IG distribution for a 5-inverter chain operating at 0.3 V is presented. For this case, the Monte-Carlo simulations have used a uniform distribution of supply voltage and Process Variation (PV). Even for this case, the IG distribution exhibits accurate modeling capabilities.

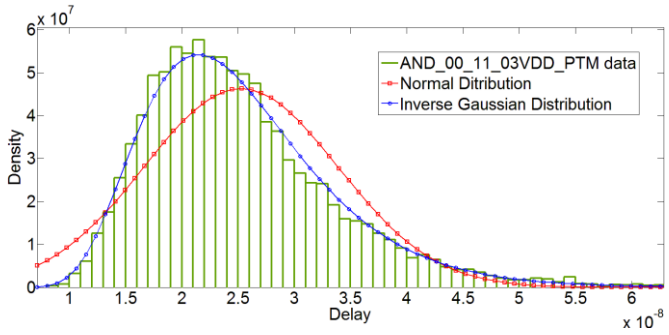


Figure 4-1: Inverse and Normal Gaussian Distribution Fitting (2-input AND @ Vdd= 0.3V).

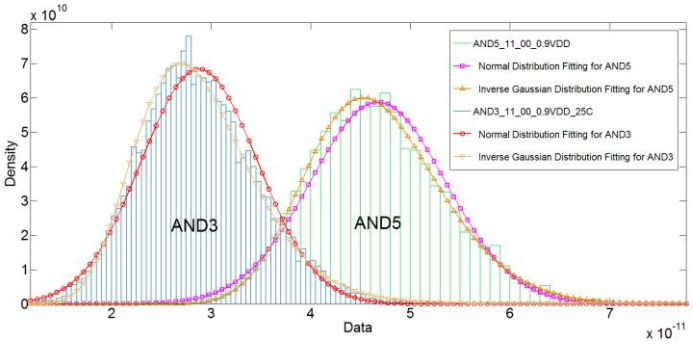


Figure 4-2: 3-AND and 5-AND Gates Chain Inverse and normal Gaussian Distribution (@ Gaussian Distribution of Vdd and PV).

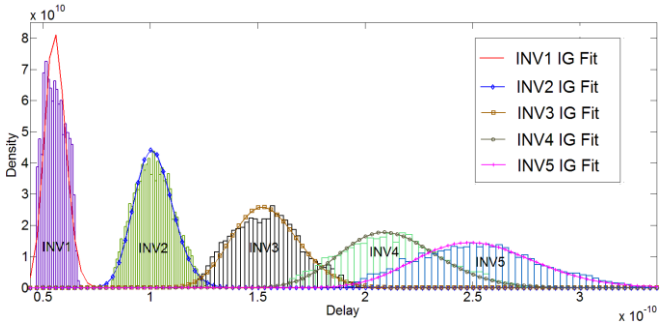


Figure 4-3: 5-Inverter Chain Inverse Gaussian Distribution (@ Gaussian Distribution of Vdd and PV).

Therefore, the IG distribution provides better delay distribution models for nominal, near, and sub threshold supply voltages with respect to the Gaussian distribution used in **[Zaynoun12].**

4.3. Model Scalability

In this subsection, we investigate the scalability of the IG using a linear composition. The linearity of the IG based composition is verified for a 7-inverter chain, a 5-AND gates chain, and for a 5-bit Ripple Carry Adder (RCA). Tables 4-1, 4-2, and 4-3 display the variance of μ and λ parameters, for these cases, while Figures 4-4, 4-5, and 4-6 present the variation of these parameters.

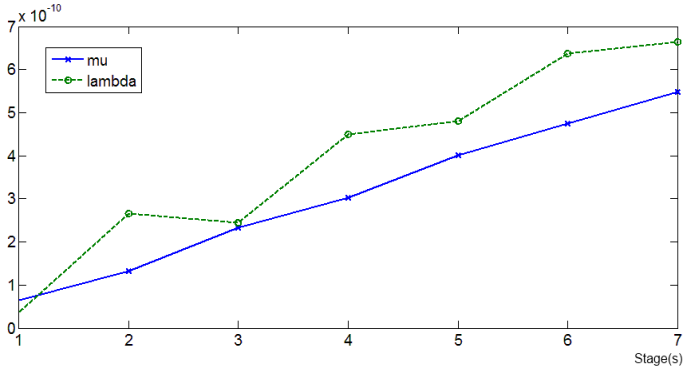


Figure 4-4: 7-Inverter Chain Inverse Gaussian Parameter Trends.

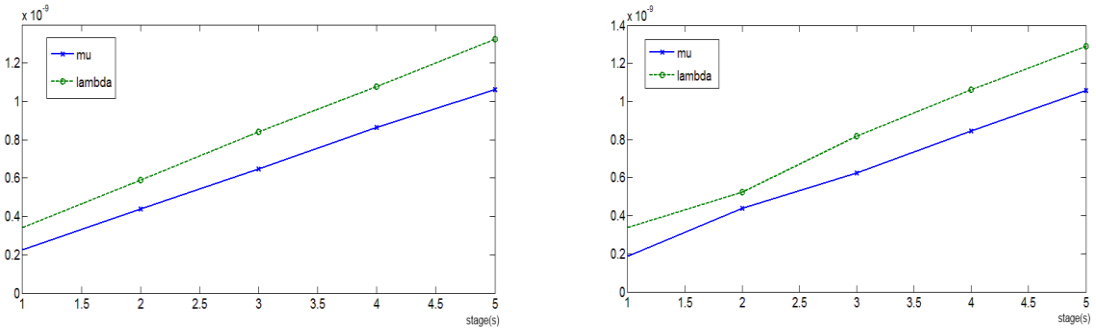
Table 4-1: μ and λ Parameters for a 7-Inverter Chain.

	Input Switch	μ (e^{-10})	Δμ(e^{-10})	λ (e^{-10})	Δλ(e^{-10})
INV1	1-0 (charging)	0.65	-	0.37	-
INV2	1-0 (discharging)	1.3	0.65	2.6	2.23
INV3	1-0 (charging)	2.3	1	2.4	-0.2
INV4	1-0 (discharging)	3.0	0.7	4.5	2.1
INV5	1-0 (charging)	4.0	1.0	4.8	0.3
INV6	1-0 (discharging)	4.7	0.7	6.4	1.6
INV7	1-0 (charging)	5.5	0.8	6.6	0.2
Average (charging)		-	0.9	-	0.1
Average (discharging)		-	0.7	-	2.0

Regarding the inverter chain, the μ parameter follows a linear evolution, while λ presents a stair wise type of increment. The λ behavior is induced by the inverter different charging and discharging delay distributions. However, λ increment only for charging and only for discharging are both linear.

For the evaluation of the 5-AND chain, the 11->10 and 11->10 input transitions have been considered. In this case, the μ and λ increments are consistent between the two input switch cases and we can observe a Figure 4-5 a linear composition for both parameters.

For the 5-bit RCA, we have considered the input switch combination, which determines propagation through the entire carry chain. The two parameters for the sum and carry bits of each full adder cell are plotted in Figure 5-6. The linear increment of the two parameters can be clearly observed in the figure.



a) b)

Figure 4-5: 5-AND Gate Chain Inverse Gaussian Parameter Trends
(Input Transition: a) 10->11 b) 11->10).

Table 4-2: μ and λ Parameters for a 5-AND Chain.

	10-11 (e^{-10})				**11-01 (e^{-10})**			
	μ	**Δμ**	**λ**	**Δλ**	**μ**	**Δμ**	**λ**	**Δλ**
AND1	2.3	-	3.4	-	1.9	-	3.4	-
AND2	4.4	2.1	5.9	2.5	4.4	2.5	5.3	1.9
AND3	6.5	2.1	8.4	2.5	6.3	1.9	8.2	2.9
AND4	8.7	2.2	10.8	2.4	8.4	2.2	10.6	2.4
AND5	10.6	1.9	13.3	2.5	10.6	2.2	12.9	2.3
Average	-	2.1	-	2.5	-	2.2	-	2.4

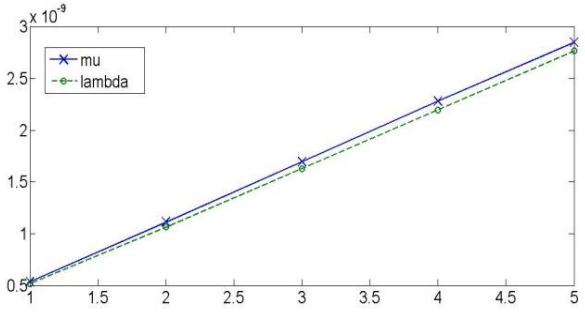


Figure 4-6: 5-bit RCA Inverse Gaussian Parameter Trends.

Table 4-3: μ and λ Parameters for a 5-bit RCA.

(e^{-10})	**Carry Switch**	**Sum Switch**	**μ**	**Δμ**	**λ**	**Δλ**
FA1	0→1	0→0	5.3	/	5.1	/
FA2	0→1	0→0	11.1	5.8	10.6	5.5
FA3	0→1	0→0	16.9	5.8	16.3	5.7
FA4	0→1	0→0	22.8	5.9	21.9	5.6
FA5	0→0	0→1	28.5	5.7	27.7	5.8
Average			-	5.8	-	5.7

4.4. Reliability Analysis with IG Distribution Model

Reliability analysis can be performed using the Cumulative Distribution Functions (CDF) of the IG distribution delay model which gives the probability of the switch to have happened at a given time, is a better metric to evaluate the correctness of the proposed model. We verify our model for a 3-input XOR and 3-bitMajority gate, and a 16-bit RCA, built from AND-Inverter configurations. The 001->101 and 011->001 input transitions have been considered for XOR and Majority gate, respectively. Table 4-4 and Figure 4-7 present the error of the analytical approach with respect to the SPICE Monte Carlo simulation of the considered circuits. For the ripple carry adder the input combination, the input sequence which causes the biggest propagation delay has been considered. Table 4-5 and Figure 4-8 present the error for the 16-bit RCA analysis with respect to the SPICE Monte Carlo simulation.

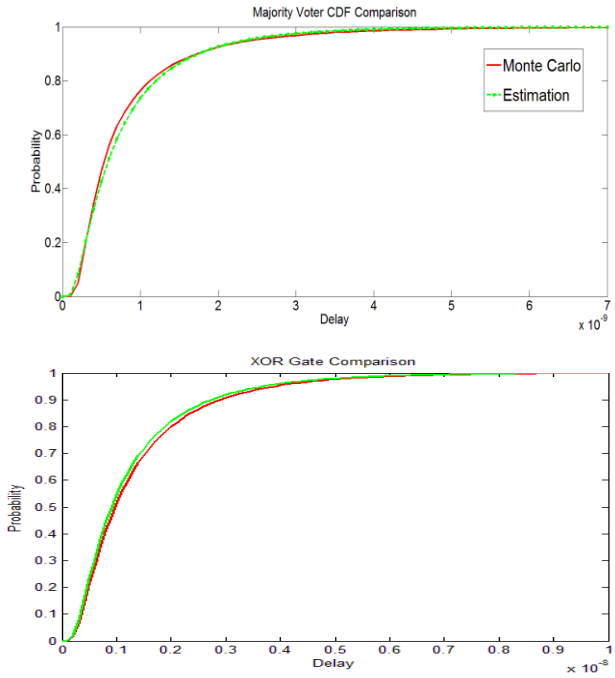


Figure 4-7: Majority gate and XOR CDF.

Table 4-4: XOR and Majority gate IG Distribution CDF Error Relative to Monte-Carlo Simulations.

Deviation	1ns	3ns	5ns	7ns	Average (0-10ns)
Majority Voter	3%	1%	0.3%	0.1%	**0.8%**
XOR	0.2%	2%	1.4%	0.7%	**1.2%**

Table 4-5: 16-bit RCA IG Distribution CDF Error Relative to Monte-Carlo Simulations.

Deviation	15ns	30ns	45ns	60ns	Average (0-60ns)
16-bit RCA	1.9%	0.6%	0.7%	0.9%	**1.7%**

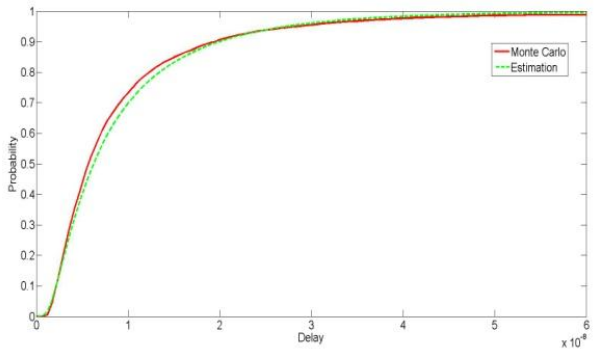


Figure 4-8: 16-bit Ripple Carry Adder CDF.

Our analysis indicates that for the considered cases the IG based model provides a good accuracy, error is less than 2%, while in most cases is smaller than 1%, which makes it a viable candidate for practical utilization in the i-RISC project context (WP 5 and WP 6).

4.5. Conclusion

This section proposed an IG distribution delay model for combinational circuits. The proposed model allows for the μ and λ parameters linear composition for the final delay PDF. We proposed to perform reliability analysis by using the CDF of the IG model and our simulations indicate that, for the considered circuits, the proposed model provides a good accuracy, the maximum error with respect to a SPICE simulation being under 2%.

The major advantage of the proposed method is its simplicity and potential scalability. Based on the IG model, fast and accurate reliability metrics (such as the CDF) can be obtained. Furthermore, for certain circuit topologies, the proposed model presents very promising scalability characteristics: a linear composition can be used in order to derive the IG distribution of the complex circuits. These properties of the proposed model make this method an ideal candidate for reliability metric estimator in synthesis tools.

5. Symbolic Analysis of Faulty Logic Gates for Uncorrelated and Correlated Errors

Abstract: In this chapter we present a method for symbolic analysis of unreliable logic circuits in the presence of correlated and data-dependent gate failures. Unlike the state-of-the-art failure models our modeling approach capture the influence of temporally signal correlation, described by Markov chains. We modified known symbolic method used for probabilistic analysis of reliable logic gates by introducing a variable substitution method, which allows us to analyze logic circuits composed of elementary faulty gates. The presented probabilistic algorithm is used for the analysis of unreliable majority and XOR gates, which are basic components of Taylor-Kuznetsov (TK) memory architectures.

Publications: S. Brkic, P. Ivanis, G. Djordjevic and B. Vasic "Symbolic Analysis of Faulty Logic Circuits in the Presence of Correlated Gate Failures", Proc. 21st Telecommunication Forum (TELFOR), Belgrade, pp 369-373,2013

5.1. Previous Work

The fundamentals of probabilistic logic circuits analysis are given in **[Parker75]**, where a so-called Parker-McCluskey method for exact signal probabilities calculation was proposed. Based on this method, signal probabilities at the outputs of logic circuit can be determined using individual gates calculation rules. Regarding the analysis of faulty probabilistic logic gates, the Parker-McCluskey method assumes a data independent error models. Other methods that use independent fault modeling include Probabilistic Decision Diagrams **[Abdollahi07]**, Four-Event **[Asadi05]** and Trigonometric Probability Calculation **[Yu11]**. Methods that use data dependent models include Bayesian networks **[Rejimon05]** and Probabilistic Transfer Matrix approach **[Krishnaswamy08]**. Both algorithms consider that only current input values influence the error occurrence; thus, the input switching is not taken into account.

5.2. Markov Chain Based Data Dependent Fault Modeling Analysis

Two types of error model analysis methods have been devised: the output dependence error model and the input dependence error model. The output dependence error model takes into account the current output $O(k)$ and the M previous outputs $O(k-1)$, $O(k-2)$..., $O(k-M+1)$. The input dependence error model for 2-input gates takes into account the current input $I1(k)$, $I2(k)$ at the gates and the M previous inputs $I1(k\text{-}1)$, $I2(k\text{-}1)$, …, $I1(k\text{-}M\text{+}1)$, $I2(k\text{-}M\text{+}1)$. Based on the obtained circuit level analysis, both models take into account current data (input or output) and previous data. Figure 5-1 presents the Markov chain for the output dependence error model for a NAND gate.

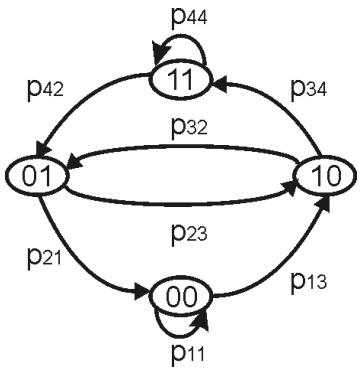


Figure 5-1: Output Dependence Error Model Markov Chain.

The input dependence model is much more complex with respect to the output dependence model: the number of states in the Markov chain grows exponentially with the number of inputs (16 states for 2 inputs, 64 states for 3 inputs, 256 states for 4 inputs). However, the input dependence model can accurately model the probabilistic fault model behavior determined by the SPICE results. Simplification in the Markov chain can be made for transitions having an error probability equal to 0 (this corresponds to the input combinations which do not lead to output switch).

5.3. Variable Substitution Method

The proposed symbolic algorithm for faulty gates analysis combines Parker-McCluskey **[Parker75]** algorithm with the date-dependent failure model given in eq. 6.1. We use the probability that signal value at the output of a 2-input faulty logic gate is equal to '1', which is given by the following equation.

$$P_{out} = \sum_{i=1}^{N} p_1^{w_1(i)} \left(1-p_1\right)^{M-w_1(i)} p_2^{w_2(i)} \left(1-p_2\right)^{M-w_2(i)} P_e\left(s_i\right) + \\ + \sum_{i=N+1}^{2^{2M}} p_1^{w_1(i)} \left(1-p_1\right)^{M-w_1(i)} p_2^{w_2(i)} \left(1-p_2\right)^{M-w_2(i)} \left(1-P_e\left(s_i\right)\right), \quad (5\text{-}1)$$

where p_1 and p_2 denote probabilities that value '1' appears at the gate inputs I1 and I2, respectively, while $w_1(i)$ and $w_1(i)$ represent, respectively, the weight of the first and second *M* bits in a binary representation of state s_i ; *N* denotes the number of states of Markov source *S* in which correct output value is equal to '0'..

The variable substitution method is developed in order to distinguish exponent originating from different time points from exponents that appear due to signal space correlation. Thus, each variable p_k (k = 1, 2) is substituted with *M* variables $p_{k,n}$, $1 \le n \le M$.

$$P_{out} = \sum_{i=1}^{N} \prod_{j=1}^{M} p_{1,j}^{s_i(j)} \left(1-p_{1,j}\right)^{\overline{s}_i(j)} \prod_{j=M+1}^{2M} p_{2,j}^{s_i(j)} \left(1-p_{2,j}\right)^{\overline{s}_i(j)} P_e\left(s_i\right) + \\ + \sum_{i=N+1}^{2^{2M}} \prod_{j=1}^{M} p_{1,j}^{s_i(j)} \left(1-p_{1,j}\right)^{\overline{s}_i(j)} \prod_{j=M+1}^{2M} p_{2,j}^{s_i(j)} \left(1-p_{2,j}\right)^{\overline{s}_i(j)} \left(1-P_e\left(s_i\right)\right), \quad (5\text{-}2)$$

The variable substitution is performed by parent-children principle – at every level of substitution parent variable is substituted with *M* children variables. After parent-children substitution, Parker-

McCluskey reduction can be applied for suppressing exponents. Finally, in the final expression we will have the probabilities associated with combinational circuit inputs.

In asymmetric paths in the circuit, the variables from different levels of substitution may appear in final expressions. Suppression is applied to all parent variable influences when they are multiplied with children variables originated from that parent. For example, the factor $p_i \cdot p_j \cdot p_{i,1} \cdot p_{i,11}$ reduces to $p_i \cdot p_j$.

5.4. Case Studies: Multiple Inputs Majority Logic and XOR Gates

We have analyzed Majority and XOR gates with multiple inputs composed out of NAND gates using the proposed method. Regarding the error probabilities, we have considered the NAND error probability dependent on the weight of each state in the Markov chain (which is equal to number of ones). We have used the following equation for expressing the error probability:

$$P_e(s_i) = \Pr\{e=1 \mid s_i\} = A_i \Pr\{e=1 \mid s_0\}, \quad 1 \le i \le 2^{2M}, \tag{5-3}$$

where A_i represent the scaling coefficients, dependent of state s_i, given by the following equation:

$$A_i = 1/p^{w(i)}, p \ge 1, \tag{5-4}$$

We have made analysis for different p, and for two probabilities of 1 at the inputs (P1 = 0.5 and P2 = 0.9). Figure 5-3 shows the failure rate of a 3-input Majority gate while. Figure 5-4 depicts results for multiple inputs Majority gates (2, 3, 4) with different input probabilities. Figure 5-5 and 5-6 show the results for 3-input XOR and for 3, 4, and 5 input XOR gates, respectively.

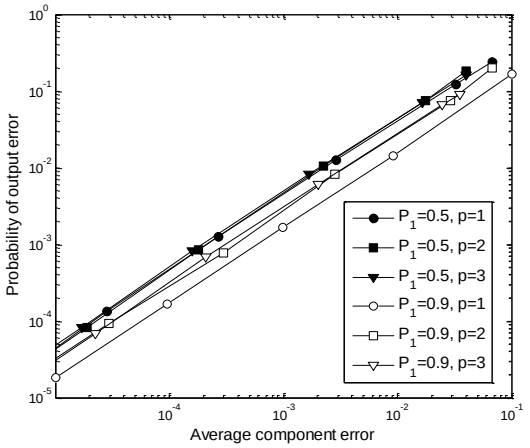


Figure 5-2: 3-input Majority Gate Output Error Probability.

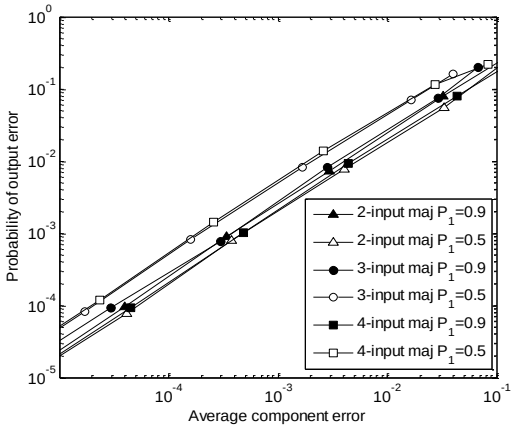


Figure 5-3: 2, 3, 4-input Majority Gates Output Error Probability for p=2.

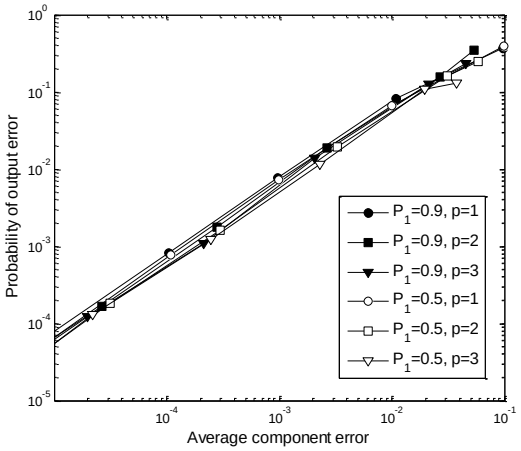


Figure 5-4: 3-input XOR Gate Output Error Probability.

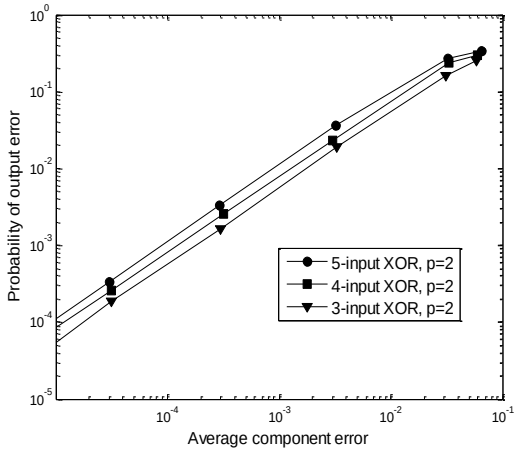


Figure 5-5: 2, 3, 4-input XOR Gates Output Error Probability for p=2.

The output error probability of 3-input Majority gate dependence of average component failures is presented in Figure 5-2, for several values of parameter *p* (=1, 2, 3) and two input probabilities *P1* = 0.5 and *P1* = 0.9. A majority gate output is equal to 1, if half or more inputs are equal to 1. Thus, when ones and zeros appear at the gate inputs with equal probabilities (*P1* = 0.5) more gate output values will be faulty, compared to case when almost all inputs are 1 (*P1* = 0.9). When *P1* = 0.5, the parameter p, which describes presented Markov model, does not have any impact on the circuit performance, while the performances differ when *P1* = 0.9. The performance comparison of Majority gates with different number of inputs is presented in Figure 5-3, when *p* = 2. It can be noted that the 2-input Majority gate has the lowest output error probability when *P1* = 0.5. However, when *P1* = 0.9, the gate with largest number of inputs (4-input gate) outperforms other logic gates.

The data-dependence does not influence greatly on the probability of error at the output of 3-input XOR gate, as illustrated in Figure 5-4. This phenomenon is a consequence of the more symmetric circuit topology in which all error states are approximately equally likely. Performance of XOR gates with 3, 4 and 5 inputs are presented in Figure 5-5. It can be noted that increasing the number of

inputs causes higher output error probability. In XOR logic circuit with more inputs, there are more gate failure combinations that may generate an output error.

5.5. Conclusion

We have developed a symbolic method for reliability analysis based on Markov chains, which suits the probabilistic behavior at sub and near threshold supply voltages. Two types of models can be used: the output dependence error model and the input dependence error models. For the input dependent error model, we have developed a variable substitution method for circuit analysis. The most important advantage of the proposed method is represented by the modeling of the data dependency. This way, with respect to the state of the art, we can perform accurate symbolic reliability analysis. However, this accuracy is obtained by sacrificing the scalability, especially for the input dependence error model.

6. General Conclusions and Next Steps

The results obtained during the project's first year have highlighted the probabilistic nature of faults for sub-powered CMOS circuits. The main cause of the probabilistic behavior is the circuit's inability to switch correctly for a given delay. The circuit level analysis has highlighted the dependence between the correct switching probability and external factors (e.g., supply voltage and temperature), delay constraints, and input data values and transitions.

Based on the circuit level analysis results, different accuracies fault models have been developed. These include simple output probabilistic (the gate has a correct output with a given probability), the probabilistic switching (the gate switches correctly with a given probability), the output dependence probabilistic model (different probabilities for different switching) and the input dependence probabilistic models (different probabilities for different input switching combinations). Having provided accurate models for probabilistic faults, taking into account input data dependence, delay constraints, and external factors as supply voltage and temperature, the first WP 2 milestone (MS2) has been reached.

The results of the first task within this work-package had been extended in three main directions:

1. **A gate level simulated fault injection methodology for combinational net-lists**. Mutant based simulated fault injection has been employed for the reliability evaluation of gate level circuit net-lists described in Verilog HDL. The proposed methodology implements the four probabilistic fault models. Our simulations of different adders configurations has proven the flexibility of the proposed fault injection method.
2. **An Inverse Gaussian delay mathematical model**. We have developed a mathematical delay model, which can accurately capture the combinational circuit behavior when operating at nominal power supply values, as well as in sub-powered regimes. Using the Cumulative Distribution Function of the proposed distribution, accurate reliability estimates (with an error less than 2 % with respect to the SPICE simulation) can be performed. Furthermore, the Inverse Gaussian model presents good scalability feature: the model for complex circuits can be derived using linear composition.
3. **A data dependent symbolic analysis method based on Markov chains**. The proposed methodology represents the first approach to perform symbolic reliability analysis, which takes into consideration data dependencies. Markov chains for output data dependence and for input data dependence have been developed.

Regarding future WP 2 work, the following directions will be followed:

- Simulated Fault Injection (SFI)
    - Gate level simulated fault injection for sequential elements (using a mutant approach) and interconnects (using saboteurs),
    - Register Transfer Level (RLT) based SFI,
    - FPGA probabilistic fault emulation.
- Inverse Gaussian delay modeling
    - Refinement of the IG delay model for standard cells and circuits with reconvergent fan-out,
    - Extension to sequential circuits and interconnects.

- Markov chain modeling
    - Refinement of the method based on probabilities obtained in SPICE analysis,
    - FPGA acceleration to address the scalability problem.

Furthermore, we aim at extending the proposed circuit level analysis in order to derive energy measures and energy profiles for CMOS circuits at sub- and near-threshold operation conditions.

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