Research reported in this presentation was supported by the EU-FP7 Programme, under Grant Agreement 309129 (i-RISC project).

The analysis of Taylor-Kuznetsov fault-tolerant memories under correlated gate failures

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Introduction

- It is widely recognized that decreasing transistor size can produce many advantages in terms of computation efficiency.
- However, energy dissipation and noise sensitivity became critical issues.
- Fault tolerance is recognized as on of the top challenges in semiconductor technology.
- Device failures can be broadly divided into three main categories: permanent, intermitted and transient.
- Transient faults are mainly due to single or multiple event upsets or timing errors, and have probabilistic behavior.

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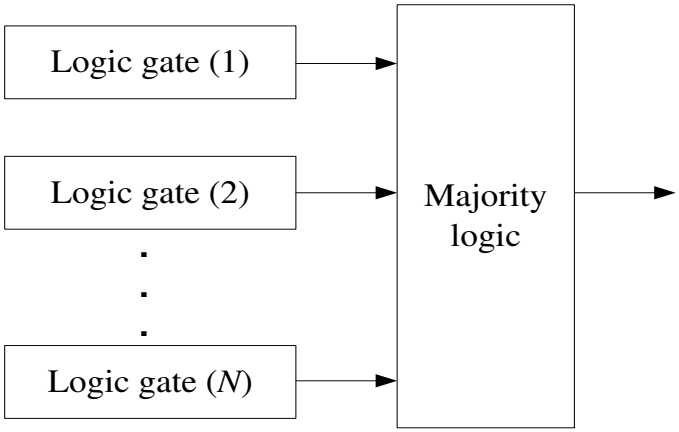
Von Neumann's approach to fault-tolerance

- The conventional approach to deal with faulty gates is to make them reliable by multiplexing.
- Von Neumann's architecture corresponds to a repetition coding technique.
- Although multiplexing has the advantage of simplicity, it leads to extremely large hardware redundancy when gate reliability is small.



[1] J. Von Neumann, "Probabilistic Logics and the Synthesis of Reliable Organisms from Unreliable Components", in C. E. Shannon and J. McCarthy, Eds. *Automata Studies*. Princeton: Princeton University Press, pp. 43-98, 1956.

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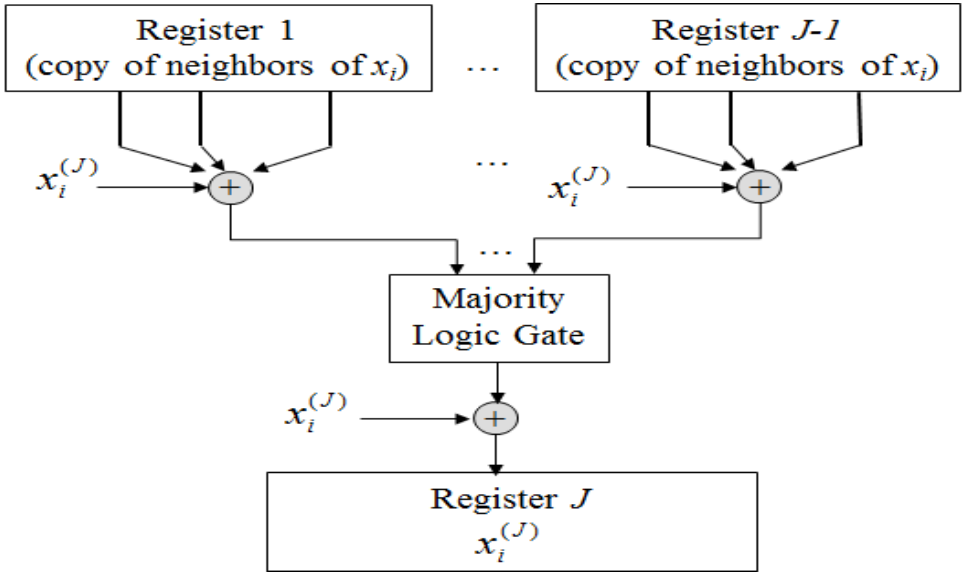
Taylor-Kuznetsov (TK) fault-tolerant system

- Use of better error correcting codes (LDPC) can improve performance of fault-tolerant systems.
- A memory built from unreliable components can achieve storage capacity C for all memory redundancies greater that $1/C$.



[2] M. Taylor, "Reliable Information Storage in Memories Designed from Unreliable Components", *Bell System Technical Journal,* 47, pp 2299-2337, 1968.

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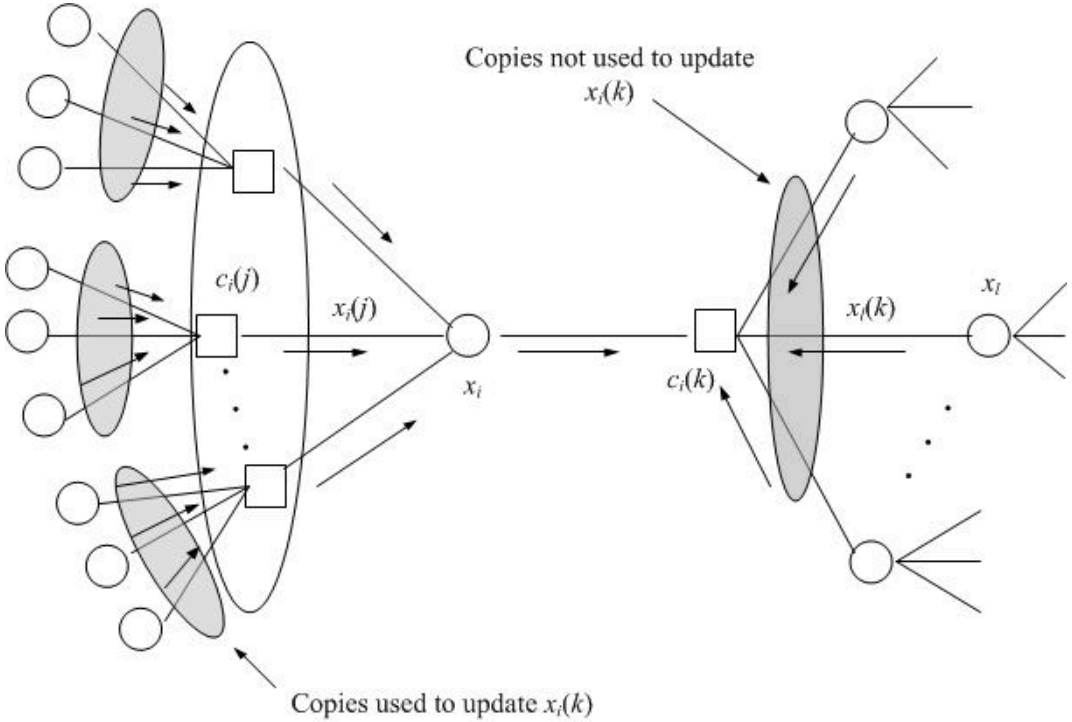
TK scheme as Gallager-B Decoding Algorithm

- Exclusion of one parity check is done by message passing principle.



[3] B. Vasic and S. K. Chilappagari, "An Information Theoretical Framework for Analysis and Design of Nanoscale Fault-Tolerant Memories Based on Low-Density Parity-Check Codes", *IEEE Transactions on Circuits and Systems I, Regular Papers*, vol. 54, no. 11, pp. 2438-2446, Nov. 2007.

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Components of TK scheme

- TK scheme is composed of, memory elements, multi-input XOR gates, majority logic gates and 2-input XOR gate.
- Every logic gate in TK scheme can produce an error.
- Multi-input gates are modeled as digital scheme composed of 2-input Boolean functions.
- Original TK scheme was examined in the presents of uncorrelated (Von Neumann type of) errors.
- We analyzed component of TK scheme when, due to noise influence to chips with sub-threshold voltages, error correlation at the output of logic gates exist.

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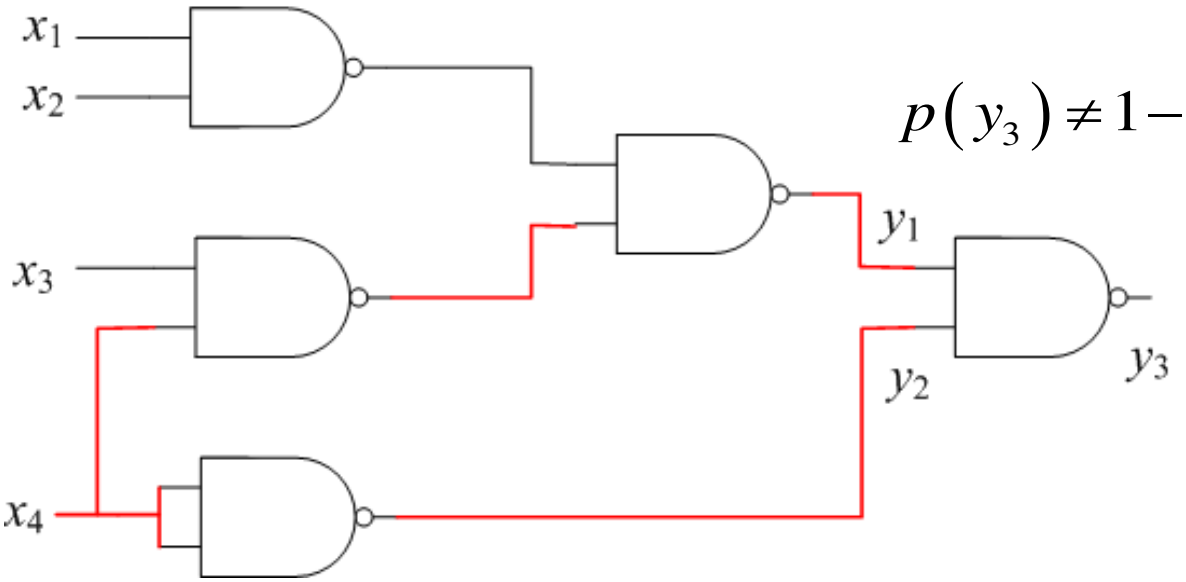
Probabilistic analysis of digital circuits

- The signal probability $p(x)$ of a logic signal x indicates the likelihood that signal x is equal to 1.
- Major challenge of probabilistic analysis is dealing with signal correlation.

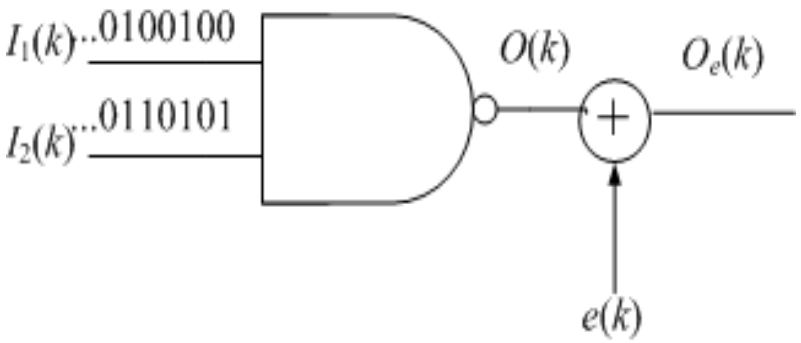


$$p(y_3) \neq 1 - p(y_1)\,p(y_2)$$

[4] K. P. Parker and E. J. McCluskey: "Probabilistic treatment of general combinational networks," *IEEE Trans. Comput., vol. C-24, pp. 668-670, 1975.*

Research reported in this presentation was supported by the EU-FP7 Programme, under Grant Agreement 309129 (i-RISC project).

Analytical methods for faulty logic gates analysis



$$O_e(k) = xor(O(k) + e(k)), k > 0.$$

- Two soft-error types: unconditional and conditional.
- Unconditional error model – probability of error is constant (PDD, Four-Event, TPC...)
- Conditional error model – probability of error is data-dependent (Bayesian networks, PTM approach...).

[5]T. Rejimon and S. Bhanja: "Scalable probabilistic computing models using Bayesian networks," *Proc. Midwest Symp. Circuits & Syst., pp. 712-715, 2005.*

[6] S. Krishnaswamy *et al.:* "Probabilistic transfer matrices in symbolic reliability analysis of logic circuits," *ACM Trans. Design Autom. Electron. Syst., vol. 13, Article* No. 8, 2008.

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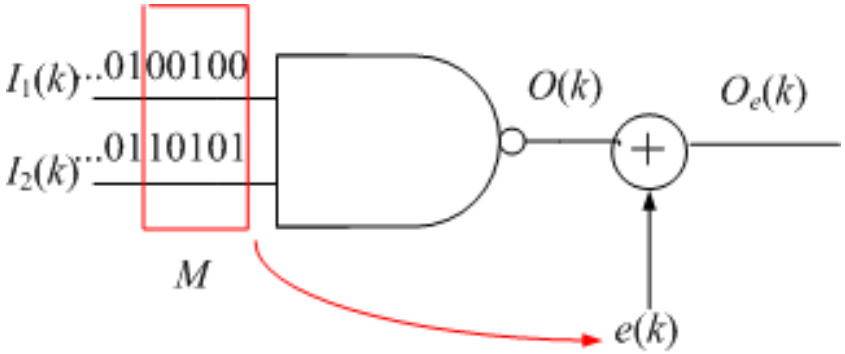
Error modelling using Markov chains (1)



$$O_e(k) = xor(O(k) + e(k)), k > 0.$$

- Error value $e(k)$ is formed based on M consecutive input values.
- Set of all possible states $S = \{s_1, s_2, ..., s_{2^{2M}}\}$.
- Every state is coded by a binary vector of length $2M$.

$$s_i = [\underbrace{b_1 \quad b_2 \quad \dots \quad b_M}_{I_1} \underbrace{b_{M+1} \quad b_{M+2} \quad \dots \quad b_{2M}}_{I_2}],$$

$$b_j \in \{0,1\}, 1 \le j \le 2M, 1 \le i \le 2^{2M}.$$

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Error modelling using Markov chains (2)

- Different error probabilities could be associated to every state: $\mathbf{P_e} = \left[P_e(s_1) \quad P_e(s_2) \quad \ldots \quad P_e(s_{2^{2M}}) \right]$.
- NAND logic gates are most sensitive to errors if both inputs are equal to zero. Consequently, all-zero state has highest and all-ones state lowest error probability.
- The weight of the state s_i, $w(i)$, defines $P_e(s_i)$.

$$P_e(s_i) = \Pr\{e = 1 | s_i\} = A_i \Pr\{e = 1 | s_0\}, \quad 1 \le i \le 2^{2M}.$$

$$A_i = 1 / p^{w(i)}, \; p \ge 1.$$

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Error modelling using Markov chains (3)

- If first N states cause output value 0 and the all other states value 1 it follows

$$P_{1,out} = \Pr\{O_e = 1\} = \sum_{i=1}^{N} P_1^{w_1(i)} \left(1-P_1\right)^{M-w_1(i)} P_2^{w_2(i)} \left(1-P_2\right)^{M-w_2(i)} P_e\left(s_i\right) + \sum_{i=N+1}^{2^{2M}} P_1^{w_1(i)} \left(1-P_1\right)^{M-w_1(i)} P_2^{w_2(i)} \left(1-P_2\right)^{M-w_2(i)} \left(1-P_e\left(s_i\right)\right).$$

  where $w_1(i)$ and $w_2(i)$ denotes the weights of first and second M bits in state s_i, respectively.
- The exponents appear as a consequence of multiple discrete times analysis and must not be suppressed.
- To preserve exponents substitution of the variables is done.

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Error modelling using Markov chains (4)

- The variable P_k (k=1,2) is substituted with M variables $P_{k,n}$, $1 \le n \le M$ and we have

$$P_{1,out} = \sum_{i=1}^{N} \prod_{j=1}^{M} P_{1,j}^{s_i(j)} \left(1 - P_{1,j}\right)^{\bar{s}_i(j)} \prod_{j=M+1}^{2M} P_{2,j}^{s_i(j)} \left(1 - P_{2,j}\right)^{\bar{s}_i(j)} P_e\left(s_i\right)$$

$$+ \sum_{i=N+1}^{2^{2M}} \prod_{j=1}^{M} P_{1,j}^{s_i(j)} \left(1 - P_{1,j}\right)^{\bar{s}_i(j)} \prod_{j=M+1}^{2M} P_{2,j}^{s_i(j)} \left(1 - P_{2,j}\right)^{\bar{s}_i(j)} \left(1 - P_e\left(s_i\right)\right),$$

  where $\bar{s}_i(j)$ denotes negation of $s_i(j)$.

- Substitution is carry out through every signal path:

$$P_1 \rightarrow \left\{P_{1,1}, P_{1,2}, \ldots, P_{1,M}\right\}, P_{1,1} \rightarrow \left\{P_{1,11}, P_{1,12}, \ldots, P_{1,1M}\right\} \ldots$$

- At the output all exponents are suppressed, and than all variables are turned back into P_1 and P_2.

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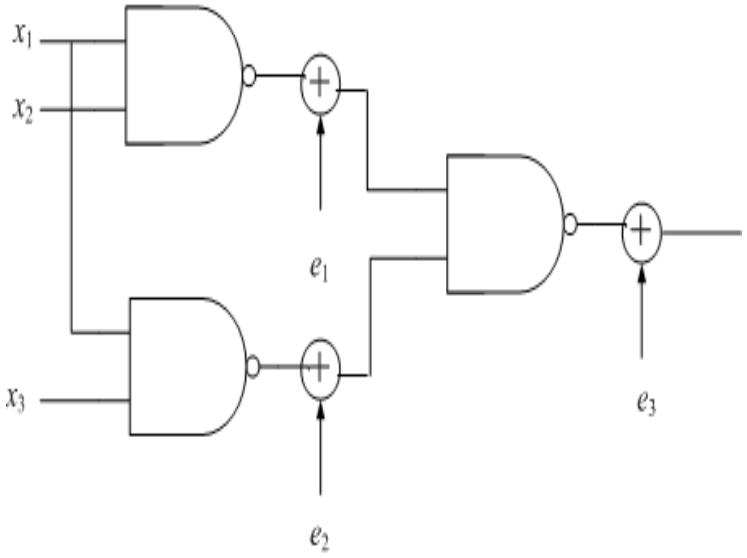
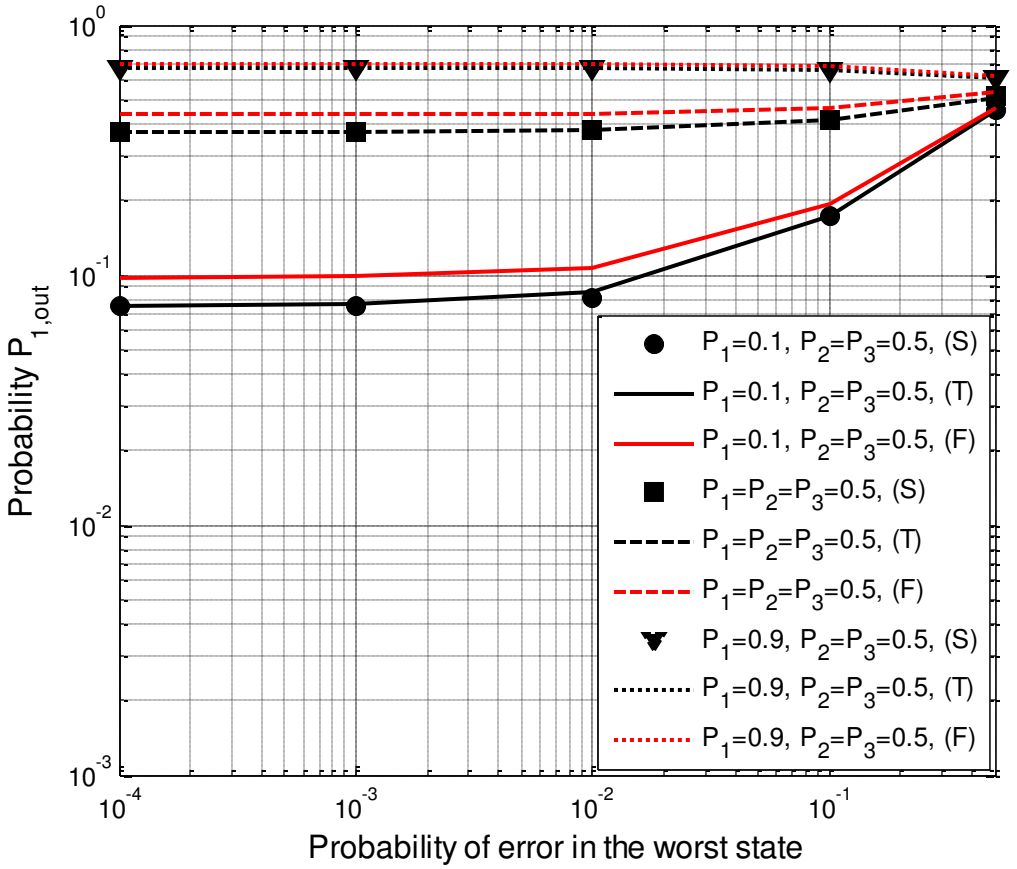
Analytical method – 3-input gate example (*M*=2, *p*=2)





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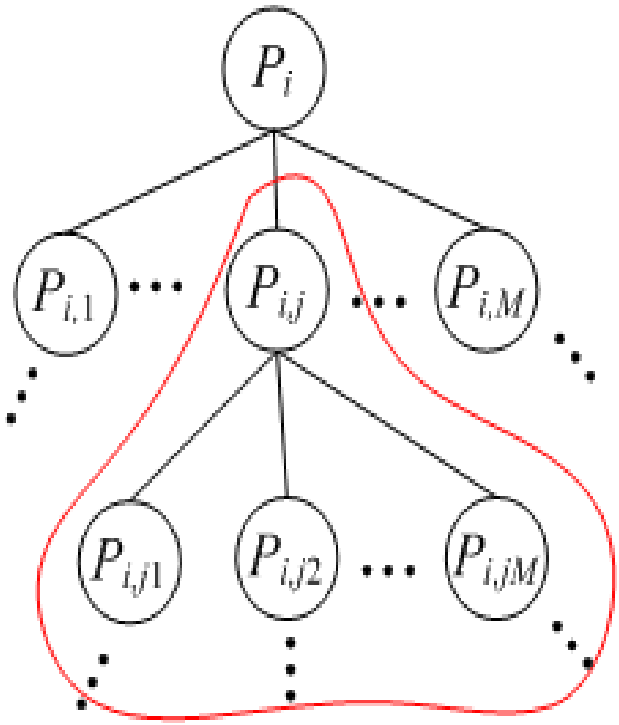
Asymmetric path analysis

- Due to asymmetric paths in the circuit, variables from different levels of substitution can appear in a final expression.

$$P_{out} = \sum_i A_i(p) P_e^{f(i)} \prod_{j=1}^{N_{in}} P_j^{a(i)} \prod_{k_1=1}^{M} P_{1,k}^{b_1(i)} \cdots \prod_{k_{N_{in}}=1}^{M} P_{N_{in},k}^{b_{N_{in}}(i)} \prod_{n_{11}=1}^{M} P_{1,11}^{c_{11}(i)} \cdots$$



- Variables from parent levels influence on all children variables.
- For example, factor $P_iP_jP_{i,1}P_{i,11}$ reduces to P_iP_j.

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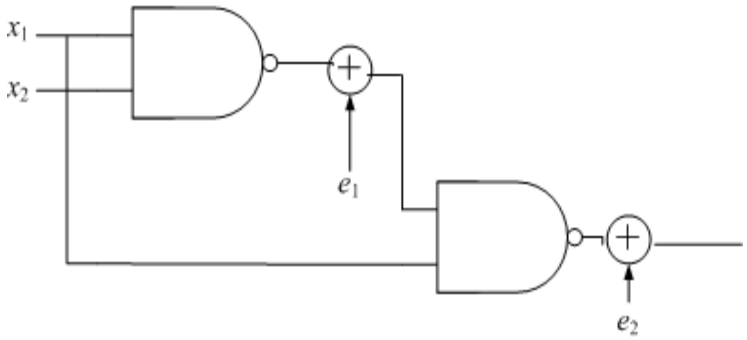
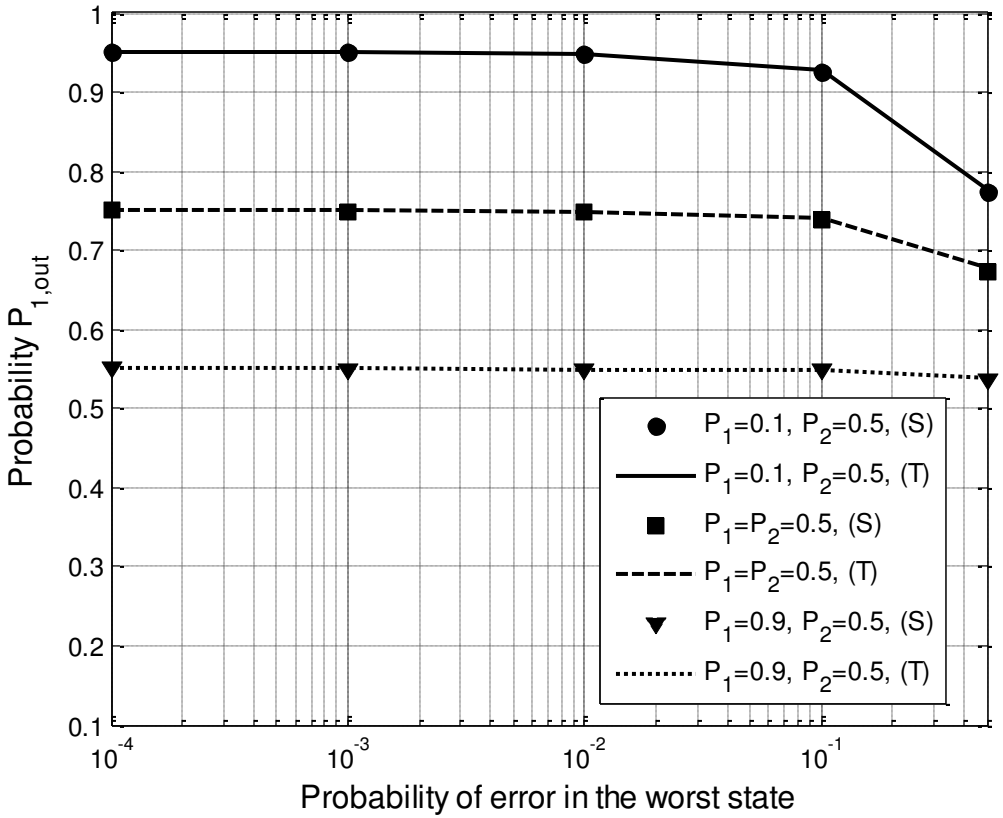
Analytical method – 2-input gate example (*M*=2, *p*=2)





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Complexity analysis

- The number of variables used in algorithm depends on number of inputs and length of correlated paths.
- N_c input ports are correlated (x_1,x_2,…,x_{Nc}), and N_{un}(=N_{in}-N_c) are independent.
- $D_i^{(j)}, 1 \le i \le N_c, 1 \le j \le N_i$, the length of the j-th path in which participate input x_i.

$$x_1 \Rightarrow D_1^{(1)}, D_1^{(2)}, \ldots, D_1^{(N_1)}$$
$$x_2 \Rightarrow D_2^{(1)}, D_2^{(2)}, \ldots, D_2^{(N_2)}$$
$$\vdots$$
$$x_{N_c} \Rightarrow D_{N_c}^{(1)}, D_{N_c}^{(2)}, \ldots, D_{N_c}^{(N_{N_c})}$$

$$N_{tot} = N_{uc} + \sum_{i=1}^{N_c} \sum_{j=1}^{N_i} M^{D_i^{(j)}}$$

Total number of variables

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Probabilistic transfer matrix (PTM) algorithm

- PTM is assigned to each logic element.

$$x \setminus y \quad \begin{matrix} 0 & 1 \\ 0 & \\ 1 & \end{matrix} \qquad I = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}$$

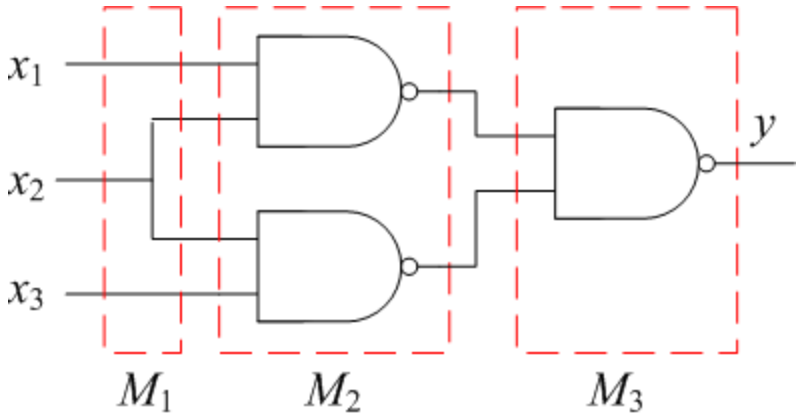
Line

$$x \setminus y_1 y_2 \quad \begin{matrix} 00 & 01 & 10 & 11 \\ 0 & & & \\ 1 & & & \end{matrix} \qquad F = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix}$$

Fanout

$$x_1 x_2 \setminus y \quad \begin{matrix} 0 & 1 \\ 00 & \\ 01 & \\ 10 & \\ 11 & \end{matrix} \qquad G = \begin{bmatrix} p_1 & 1-p_1 \\ 1-p_2 & p_2 \\ 1-p_3 & p_3 \\ 1-p_4 & p_4 \end{bmatrix}$$

NAND logic gate



$$M_1 = I \otimes F \otimes I$$

$$M_2 = G \otimes G$$

$$M_3 = G$$

$$P = M_1 \cdot M_2 \cdot M_3$$

$$p_y = p_x \times P$$

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Modified PTM algorithm (1)

- PTM of individual logic element is modified in order to analyze more general data-dependent error model.

$$x^{(k-M+1)}\ldots x^{(k-1)}x^{(k)} \setminus y \qquad \begin{matrix} 0 & 1 \end{matrix}$$

$$\begin{matrix} 00\ldots0 \\ 00\ldots1 \\ \vdots \\ 11\ldots1 \end{matrix} \qquad I' = \begin{bmatrix} 1 & 0 \\ 0 & 1 \\ \vdots & \vdots \\ 0 & 1 \end{bmatrix} \Big\} 2^M$$

Line

$$x^{(k-M+1)}\ldots x^{(k-1)}x^{(k)} \setminus y_1 y_2 \qquad \begin{matrix} 00 & 01 & 10 & 11 \end{matrix}$$

$$\begin{matrix} 00\ldots0 \\ 00\ldots1 \\ \vdots \\ 11\ldots1 \end{matrix} \qquad F' = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 1 \\ \vdots & \vdots & \vdots & \vdots \\ 0 & 0 & 0 & 1 \end{bmatrix} \Big\} 2^M$$

Fanout

NAND logic gate

$$x_1^{(k-M+1)}\ldots x_1^{(k-1)}x_1^{(k)} \mid x_1^{(k-M+1)}\ldots x_1^{(k-1)}x_1^{(k)} \setminus y \qquad \begin{matrix} 0 & 1 \end{matrix}$$

$$\begin{matrix} 00\ldots0 \mid 00\ldots0 \\ 00\ldots1 \mid 00\ldots0 \\ \vdots \\ 11\ldots1 \mid 11\ldots1 \end{matrix} \qquad G' = \begin{bmatrix} P_e & 1-P_e \\ 1-P_e/p & P_e/p \\ \vdots & \vdots \\ 1-P_e/p^{2M} & P_e/p^{2M} \end{bmatrix} \Big\} 2^{2M}$$

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Modified PTM algorithm (2)

- All tensor products are computed using modified PTMs.
- The global PTM is not computed.
- Instead, at each sublevel the distribution of output signal is determined.
- $p_1 = \left[p_{1,1}, p_{1,2}, \ldots, p_{1,2^{N_1}} \right]$ – the vector of joint distribution of all possible input combinations, where N_1 denotes number of inputs.
- p_1 is substituted with vector p_1' which contains distribution of all possible inputs in M consecutive time points

$$p_1' = \left[p_{1,1}', p_{1,2}', \ldots, p_{1,2^{N_1 M}}' \right].$$

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Modified PTM algorithm (3)

- The distribution vector at first sublevel output, p_2, can be computed as follows

$$p_2 = p_1' \times M_1,$$

where M_1 represents first sublevel PTM.

- Similarly, based on p_2 the vector p_2' which describes joint distribution of outputs in M discreet moments can be calculated

$$p_2' = \left[p_{2,1}', p_{2,2}', \ldots, p_{1,2^{N_2 M}}' \right],$$

where N_2 denotes the number of first sublevel outputs.

- Multiplications with sublevel PTMs and substitution of the level output distribution vectors continues until the circuit outputs are reached.

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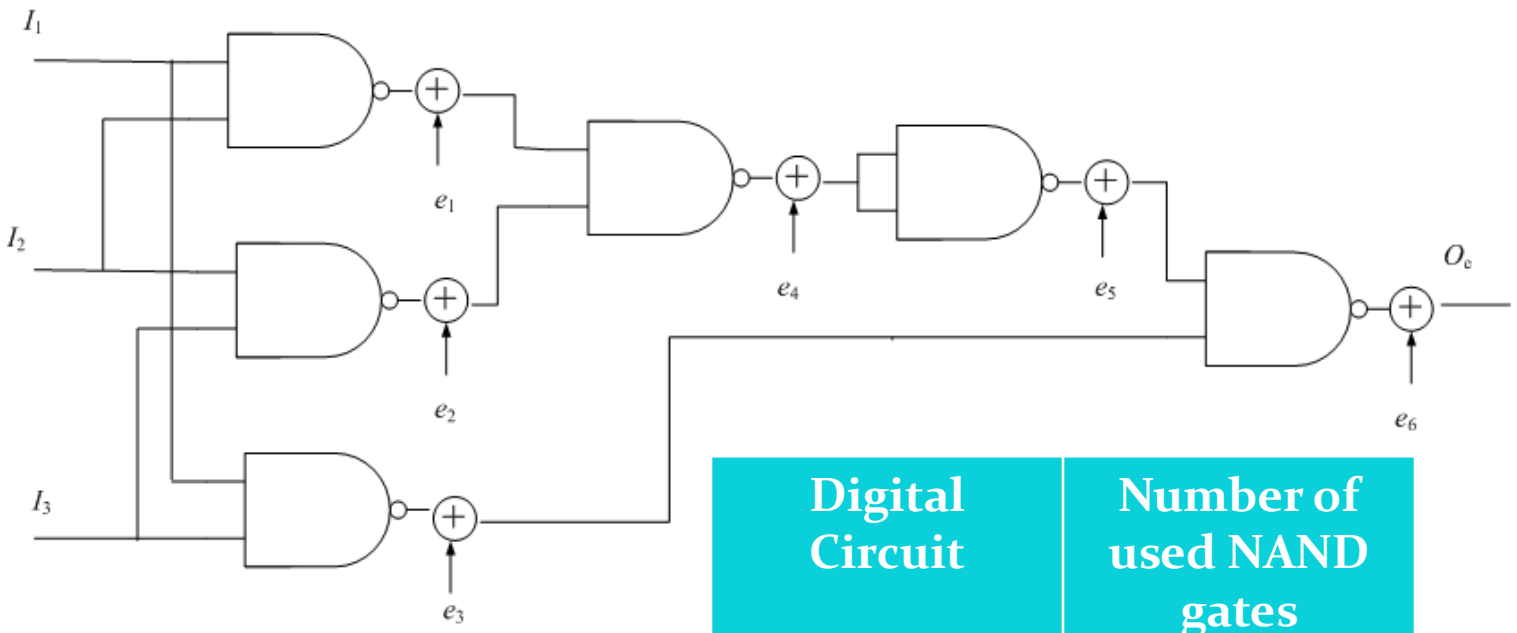
Majority logic (ML) and XOR gates



3-input majority logic (ML) gate

Digital Circuit	Number of used NAND gates
2-input ML	3
3-input ML	6
4-input ML	15
3-input XOR	10
4-input XOR	15
5-input XOR	20

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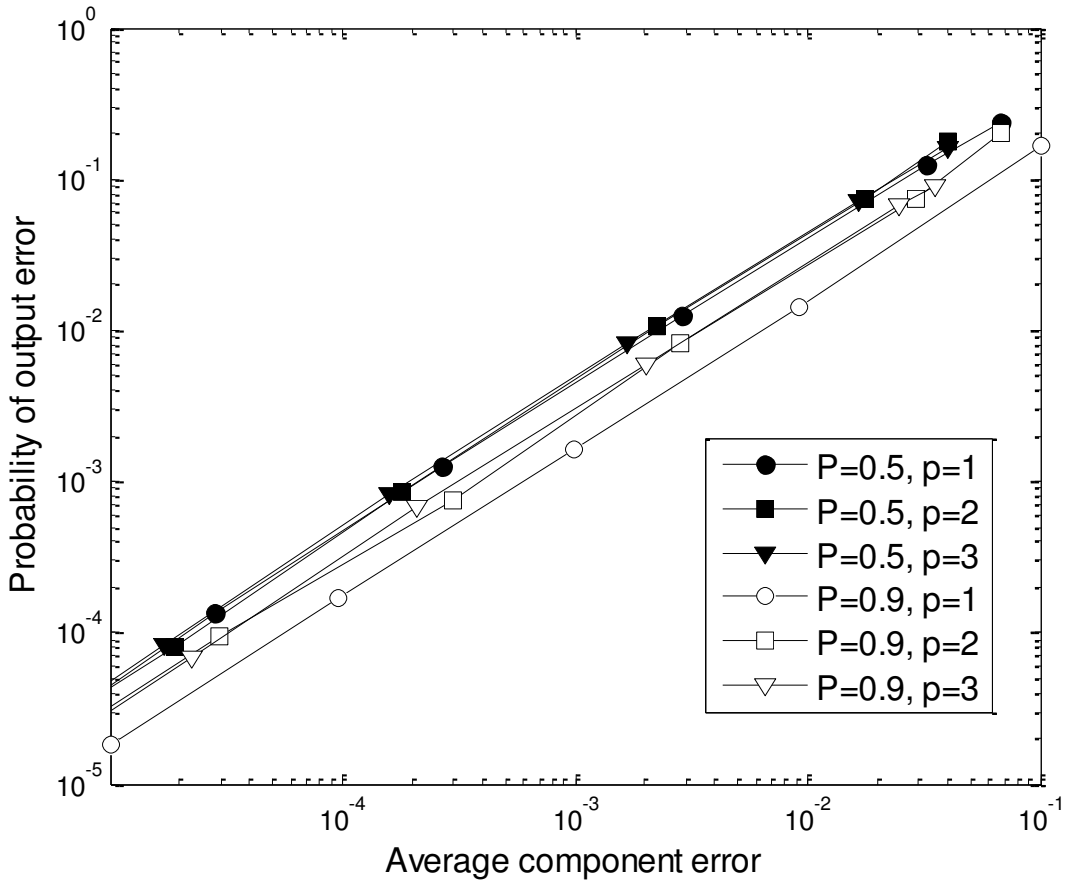
Error probability of 3-input majority logic gate

- Two values of input statistics: $P_1=\Pr\{I_i=1\}=0.5$ ($i=1,2,3$) and $P_1=0.9$, $M=2$.



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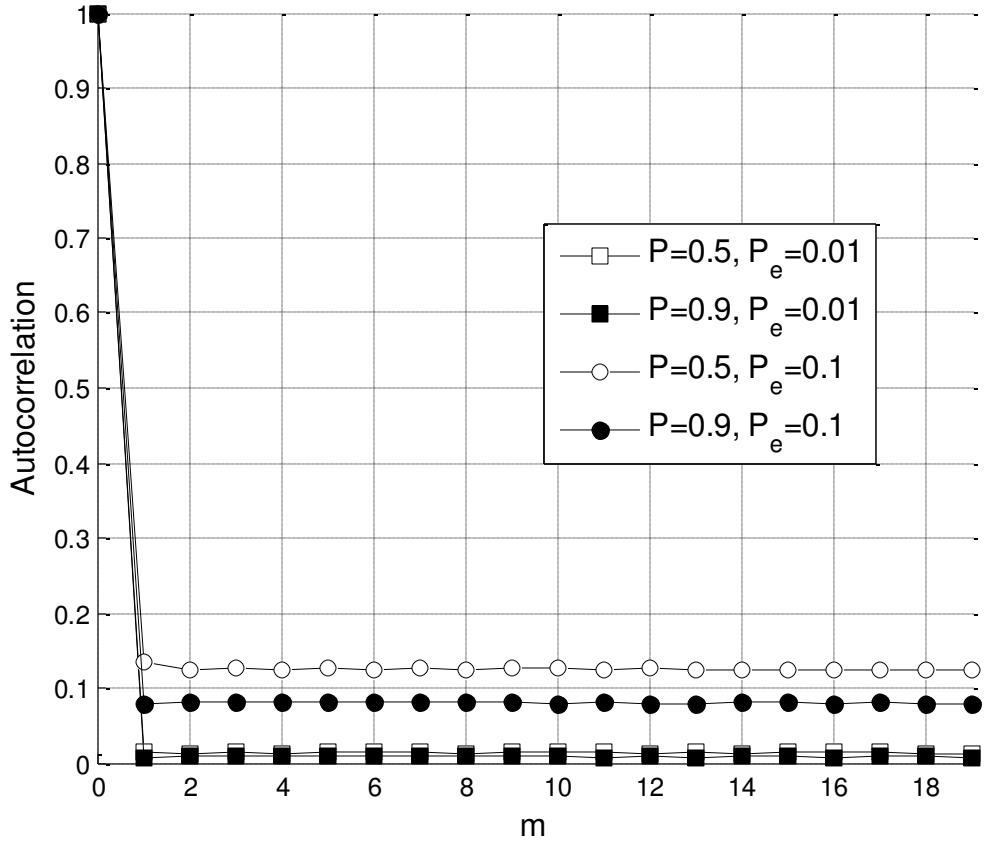
Autocorrelation function of 3-input majority logic gate

- Two values of input statistics: $P_1=\Pr\{I_i=1\}=0.5$ ($i=1,2,3$) and $P_1=0.9$, $M=2$, $p=2$.



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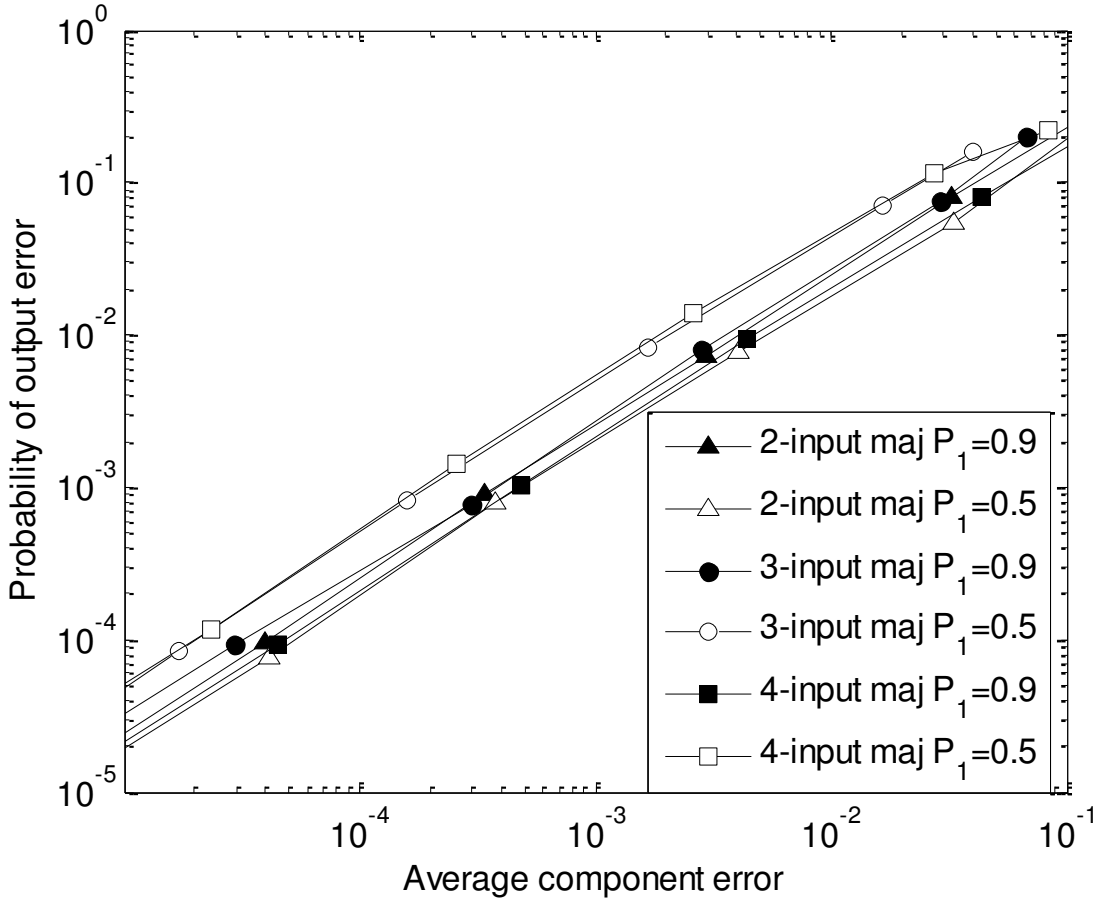
Majority logic gate with different number of inputs (M=2, p=2)



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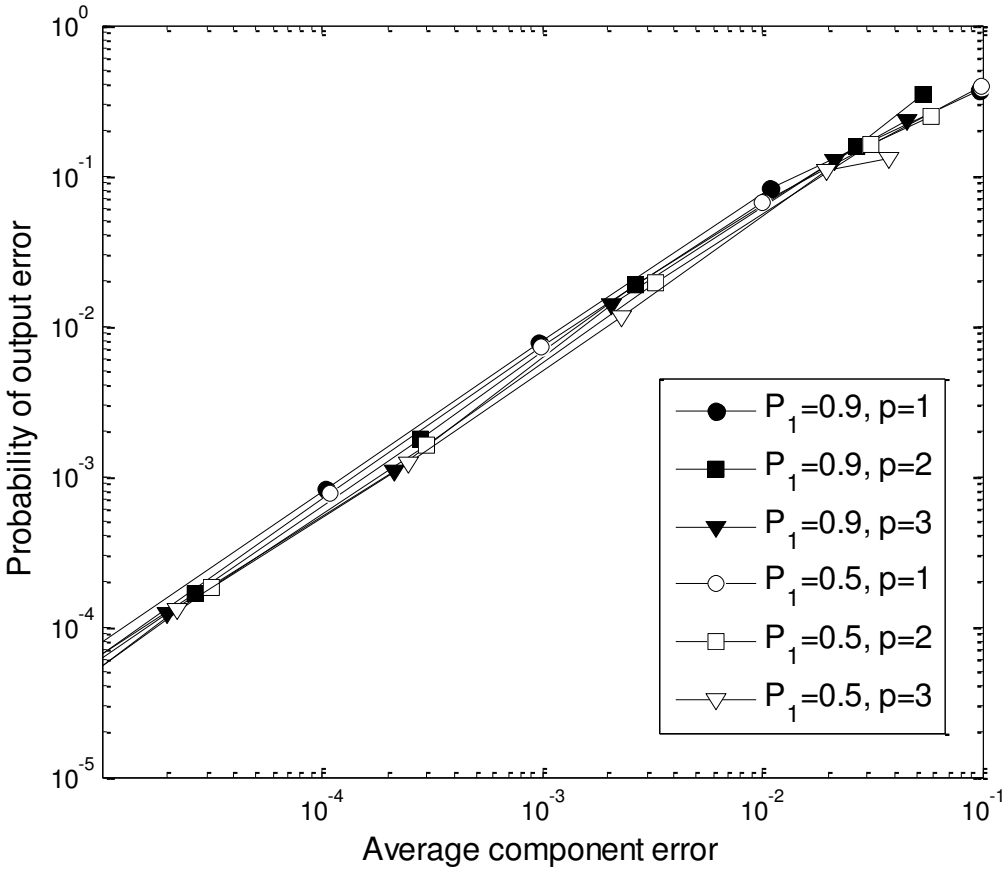
3-input XOR logic circuit performance (*M*=2)



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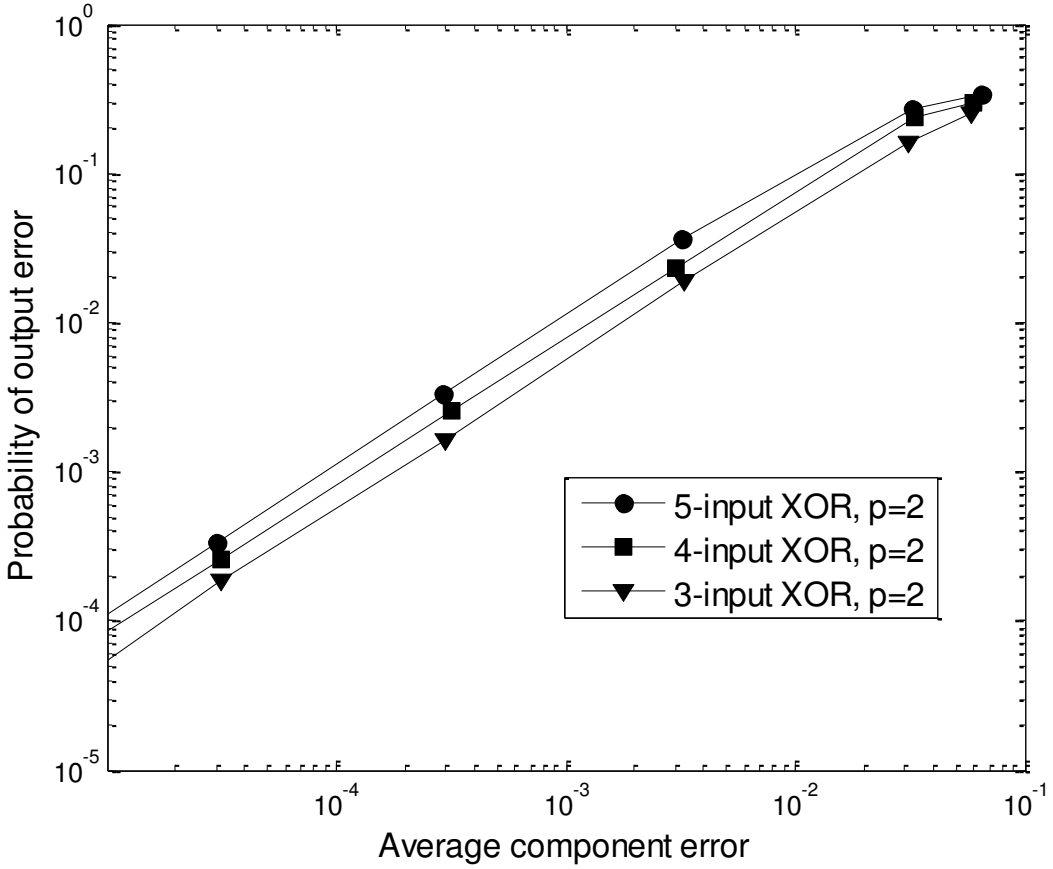
n-input XOR logic circuit performance

- Input statistics: $P_1=\Pr\{I_i=1\}=0.5$ (i=1,2,3,4,5), M=2.



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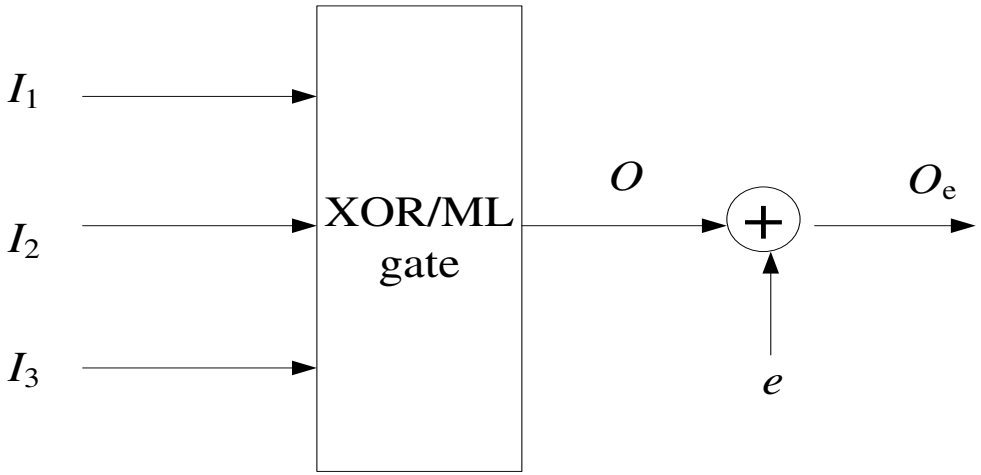
Simplification of error model

- Knowing the input statistics it is possible to form equivalent model of faulty majority logic or XOR gate.
- Faulty gate can be modeled as correct one at which output the error pattern is inserted.
- The statistical properties (average error probability and autocorrelation function) of error pattern must be unchanged.



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Conclusion

- The theoretical model for correlated error analysis in digital circuits was presented.
- The two basic components of Taylor-Kuznetsov model are examined – majority logic and *n*-input XOR gate.
- The probabilities of circuits output error obtained by this model have the similar values as in uncorrelated error model, for all cases of practical interest. Thus, simplification of error model was presented.
- Also, the similarities with uncorrelated error model are observed when autocorrelation function is derived.

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Thank you!!!