Is Boole's Computation Avenue Getting Bumpy?

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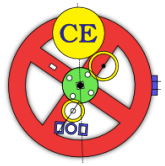
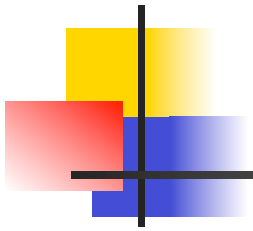
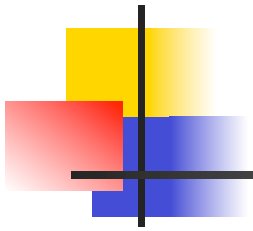




Overview

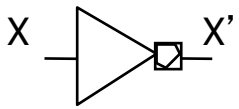
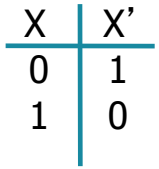
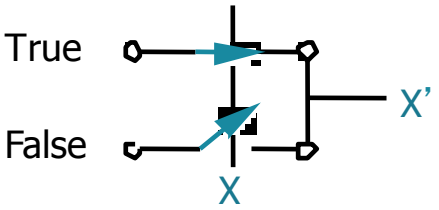
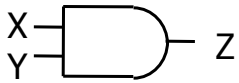
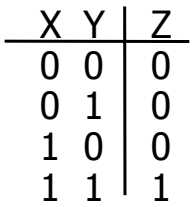
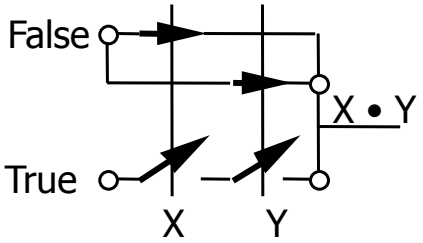
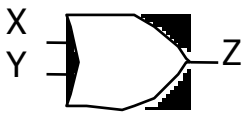
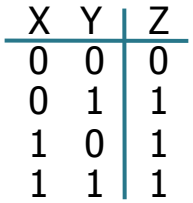
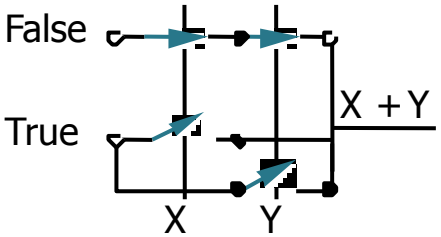
- Introduction – Boolean Algebra & Nano-Era
- Opportunities & Challenges
- Is Boolean Logic the Panacea Universalis for Digital Design?
- Is Noise our Real Enemy?
- Conclusions

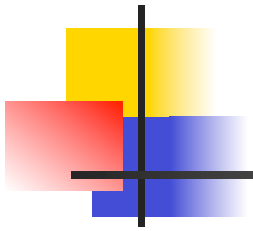


Boolean Algebra

- B = {0, 1} {false, true}
- Operations: ‘ (NOT), * (AND), + (OR)
- Properties
  - (a’)’ = a
  - a + a = a a • a = a
  - $a + 0 = a$ $a \bullet 1 = a$
  - $a + a' = 1$ $a \bullet a' = 0$
  - $a + b = b + a$ $a \bullet b = b \bullet a$
  - (a + b) + c = a + (b + c) = a + b + c
  - (a • b) • c = a • (b • c) = a • b • c
  - $a + (b \bullet c) = (a + b) \bullet (a + c)$
  - $a \bullet (b + c) = a \bullet b + a \bullet c$

Boolean Gates & Switches

Operation	*Gate*	*Truth Table*	*Switches*
NOT			
AND			
OR			

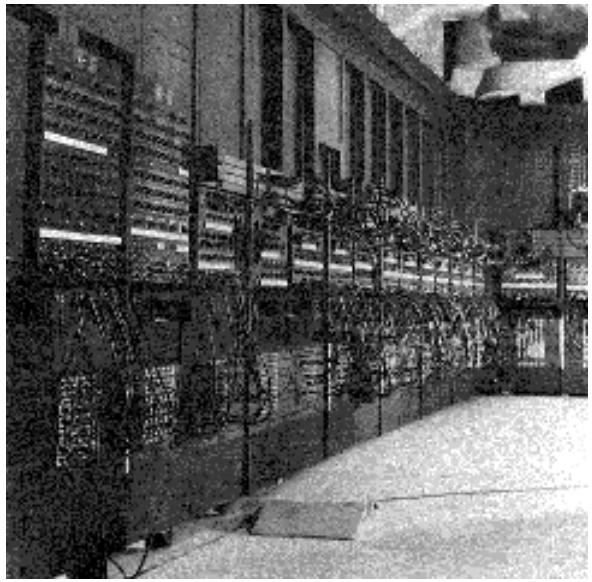


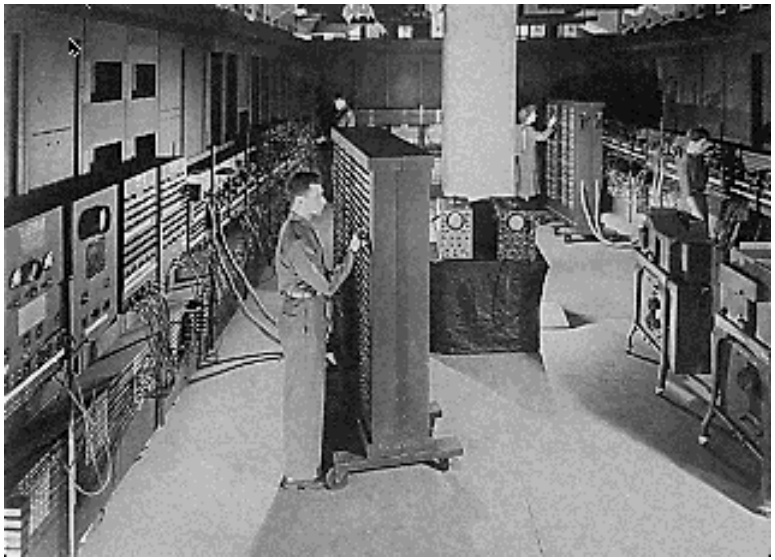
Computing Platform Basics

- Boolean logic can do all data processing.
- Functionally complete sets: NAND gates, NOR gates.
- We need wires and switches.
- Switches: Relays, Vacuum Tubes, Bipolar Transistors, Field Effect Transistors, …

Early Days: Eniac

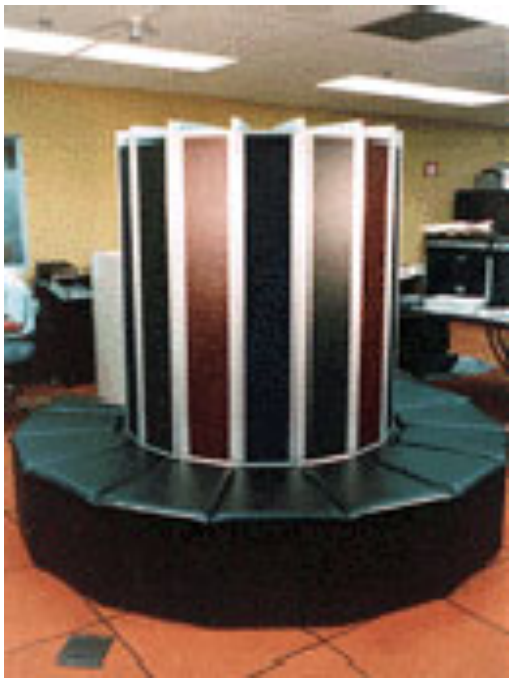
- **Used to compute ballistic trajectories.**
- **Each new problem required rewiring and setting 3000 switches.**





- 30 tons
- Consumed 200 kilowatts
- 19000 vacuum tubes

Cray



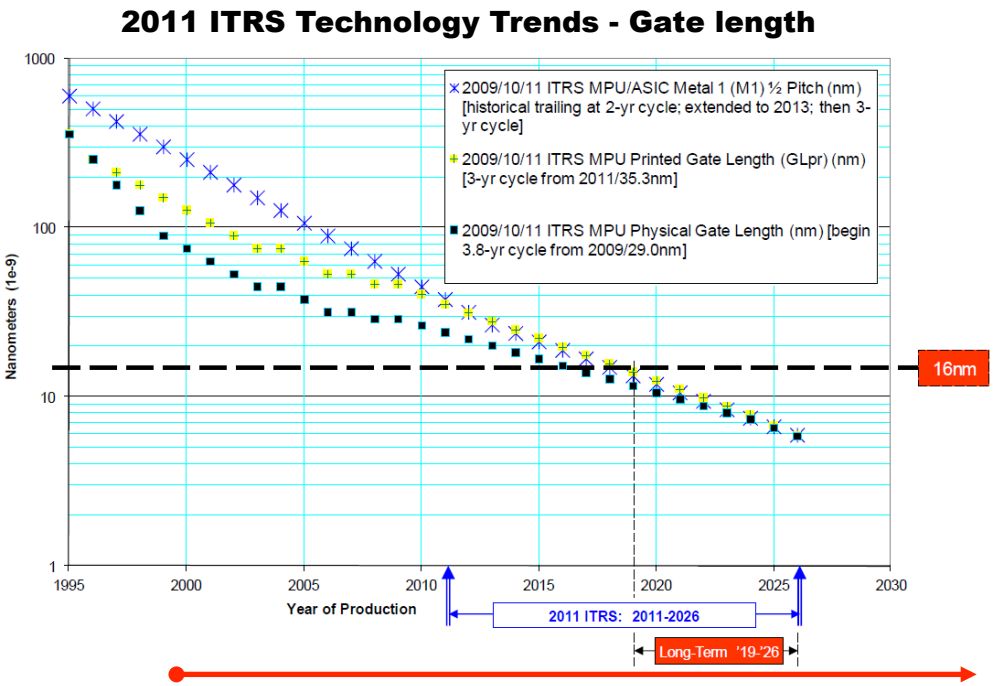
The first Cray-1® system was installed at Los Alamos National Laboratory in 1976 for $8.8 million.

It boasted a world-record speed of 160 million floating-point operations per second (160 megaflops) and an 8 megabyte (1 million word) main memory.

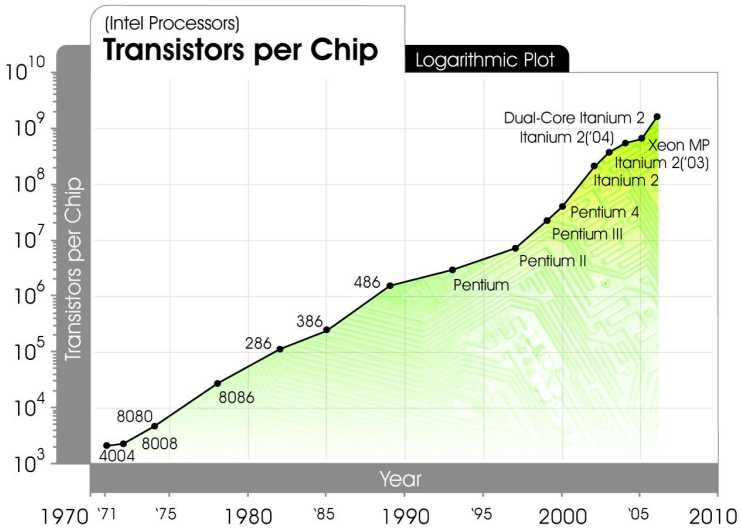
The Cray-1's architecture reflected its designer's penchant for bridging technical hurdles with revolutionary ideas. In order to increase the speed of this system, the Cray-1 had a unique "C" shape which enabled integrated circuits to be closer together. No wire in the system was more than four feet long.

To handle the intense heat generated by the computer, Cray developed an innovative refrigeration system using Freon.

Nano Era

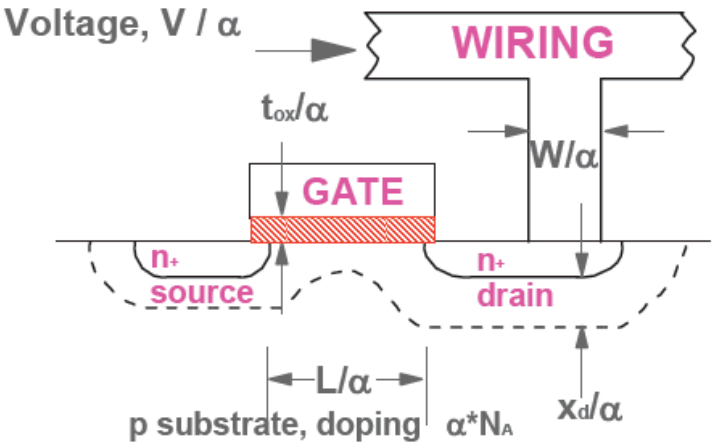


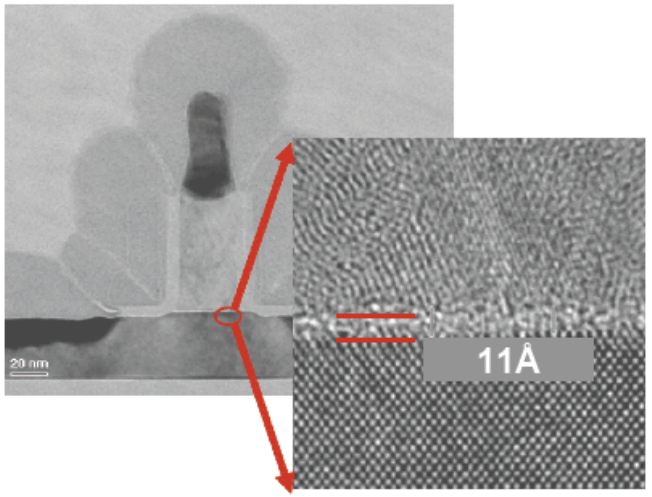
Nano Era



What Scaling Means?

CMOS Scaling Rules





SCALING:

Voltage:	V/α
Oxide:	t_{ox}/α
Wire width:	W/α
Gate width:	L/α
Diffusion:	x_d/α
Substrate:	$\alpha * N_A$

R. H. Dennard *et al.*,
IEEE J. Solid State Circuits, (1974).

RESULTS:

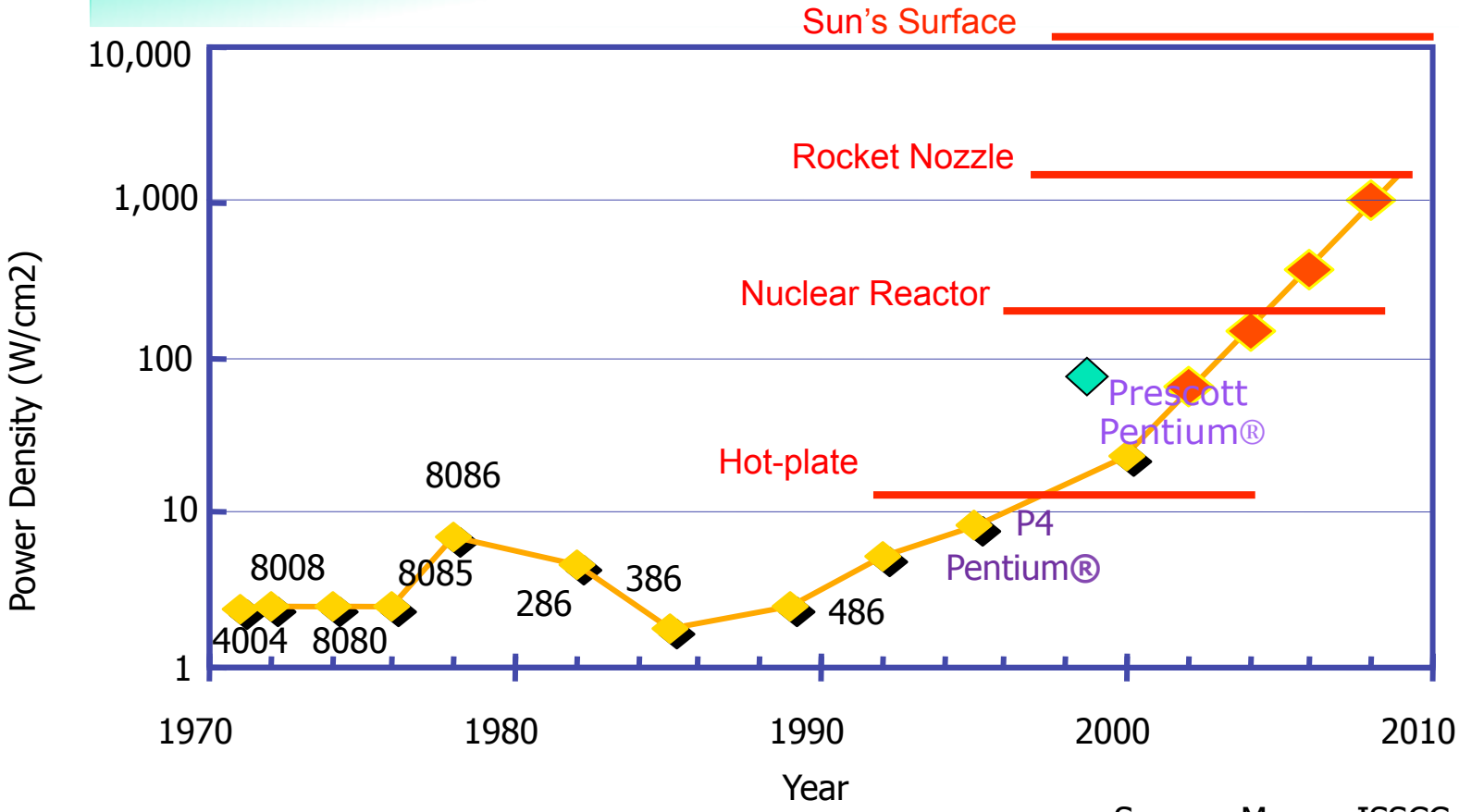
Higher Density:	$\sim\alpha^2$
Higher Speed:	$\sim\alpha$
Power/ckt:	$\sim 1/\alpha^2$
Power Density:	~~~Constant~~

- Approaching atomistic and quantum-mechanical boundaries
- **Atoms are not scalable!**

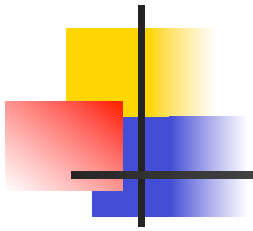
Source: T. C. Chen, IBM 2009

Power Density

Increasing power **density leads to high temperature in chip, which accelerates temperature-elevated intrinsic failure mechanisms, like NBTI.**

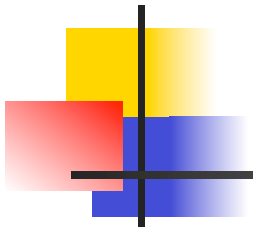


Source: Moore, ISSCC 2003



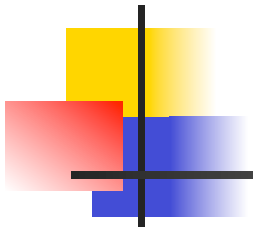
What does NANO mean?

- Deep submicron CMOS (current primary technology)
  - 90 nm, 65 nm, 45 nm, 28nm, 22nm, …
- Sooner or later MOS transistor feature size scaling ends.
- Alternative (candidate) technologies:
  - Single Electron Tunneling,
  - Resonant Tunneling Diodes,
  - Magnetic and Electron Spin Devices,
  - Carbon Nanotubes,
  - Quantum Cellular Automata,
  - Memristors, …
- As-of-yet it is not known which technology, if any, will succeed CMOS.



Opportunities & Challenges

- Increased Complexity
  - More Devices ☺
  - Difficult Design ☹
- Different Behavior
  - MOS ≠Switch
  - Alternative Devices are not Switches
- Device Unpredictability (Variability)
  - Process Parameter Variations
  - Temperature
  - Interaction
- Low Reliability
- Energy Wall



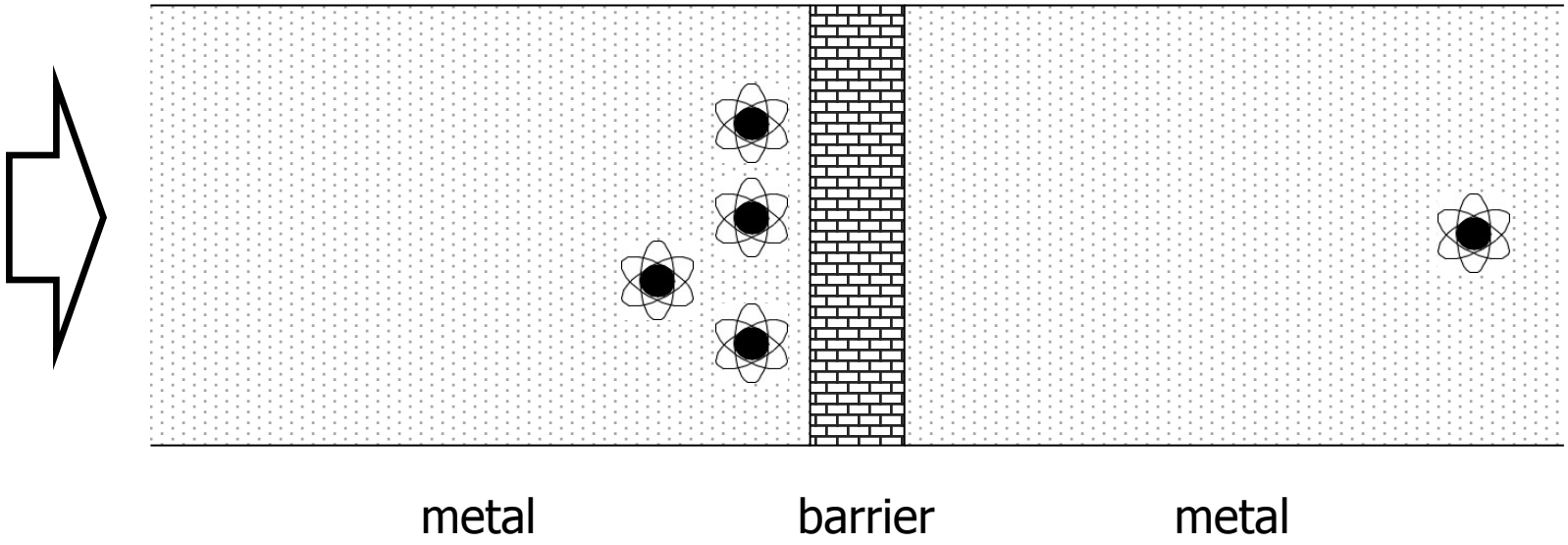
Required

- Novel Computation Paradigms
- Nano-architecture
- Design Methodologies
- Fault Tolerance
- Self Diagnosis & Repair
- Support for {R|D|P|C}bility
- Programming Models

Is Boolean Logic the Panacea Universalis for Digital Design?

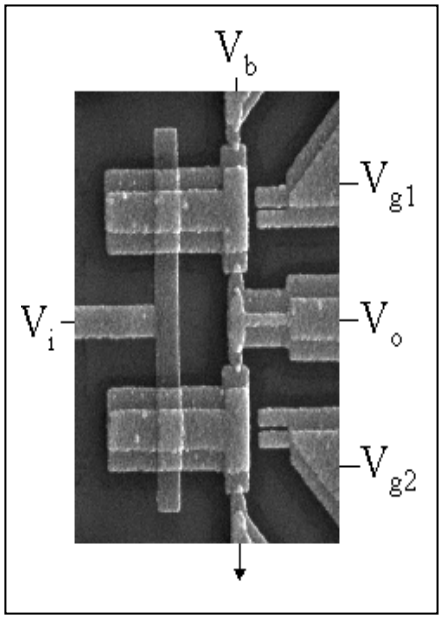
Single Electron Tunneling

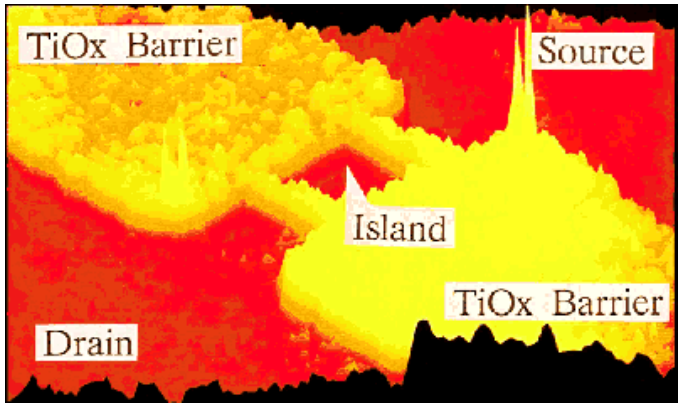
- Basic circuit element:
  - (quantum) Tunnel Junction - two (metal) conductors separated by an insulator.
- “leaking capacitor”, such that the leaking can be controlled by the voltage across the junction.

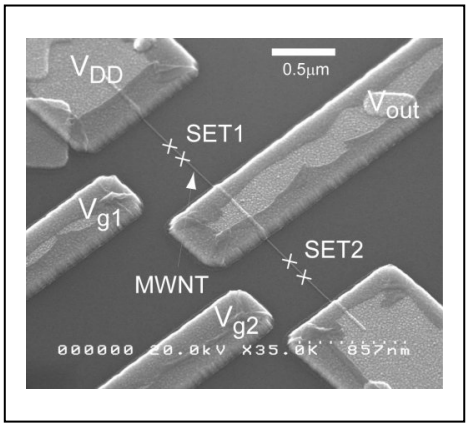


SET Junctions

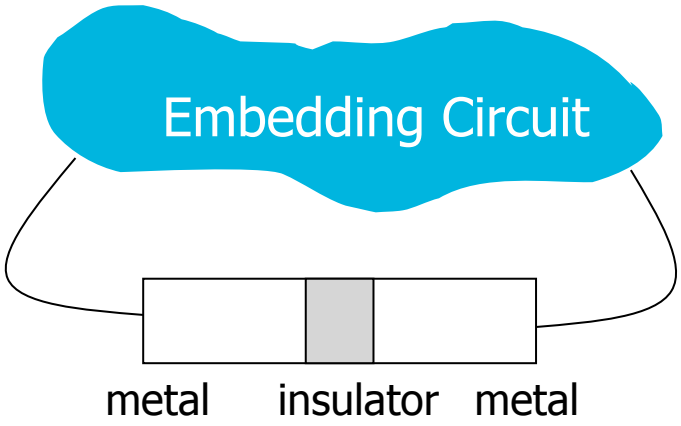
- Tunneling is a behavior.
- Tunnel junctions can be manufactured in different technologies such as:
  - Conventional lithography,
  - Patterned oxide deposition,
  - Carbon nanotubes.

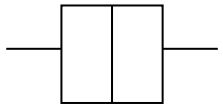






Orthodox Switching Model





symbol

We assume $P_{error} = 10^{-8}$.

Critical Voltage:

$$V_c = \frac{q_e}{2(C_e + C_j)}$$

Switching Delay:

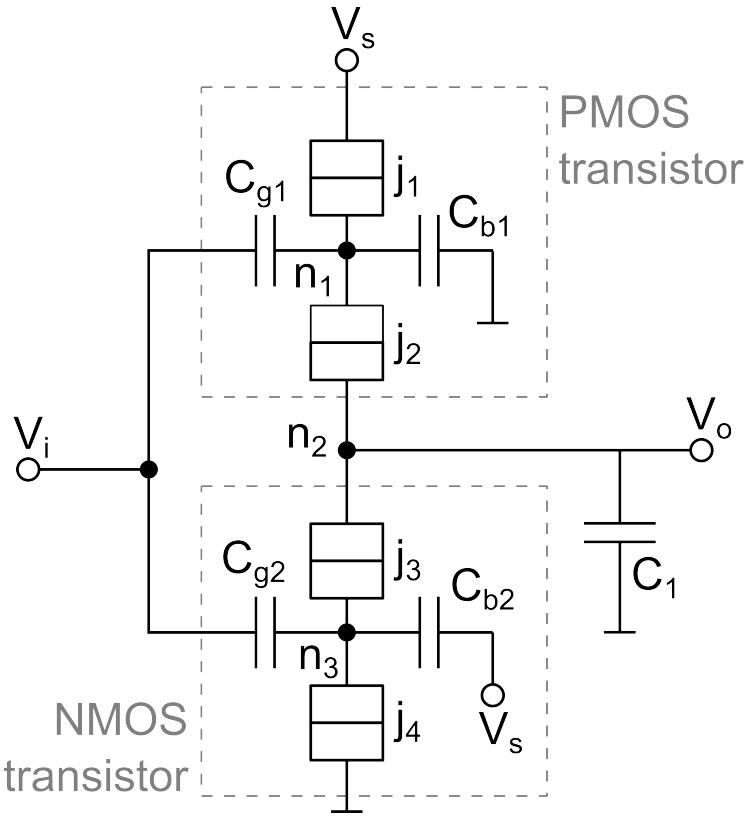
$$t_d = \frac{-\ln(P_{error}) q_e R_j}{|V_j| - V_c}$$

Energy Consumption:

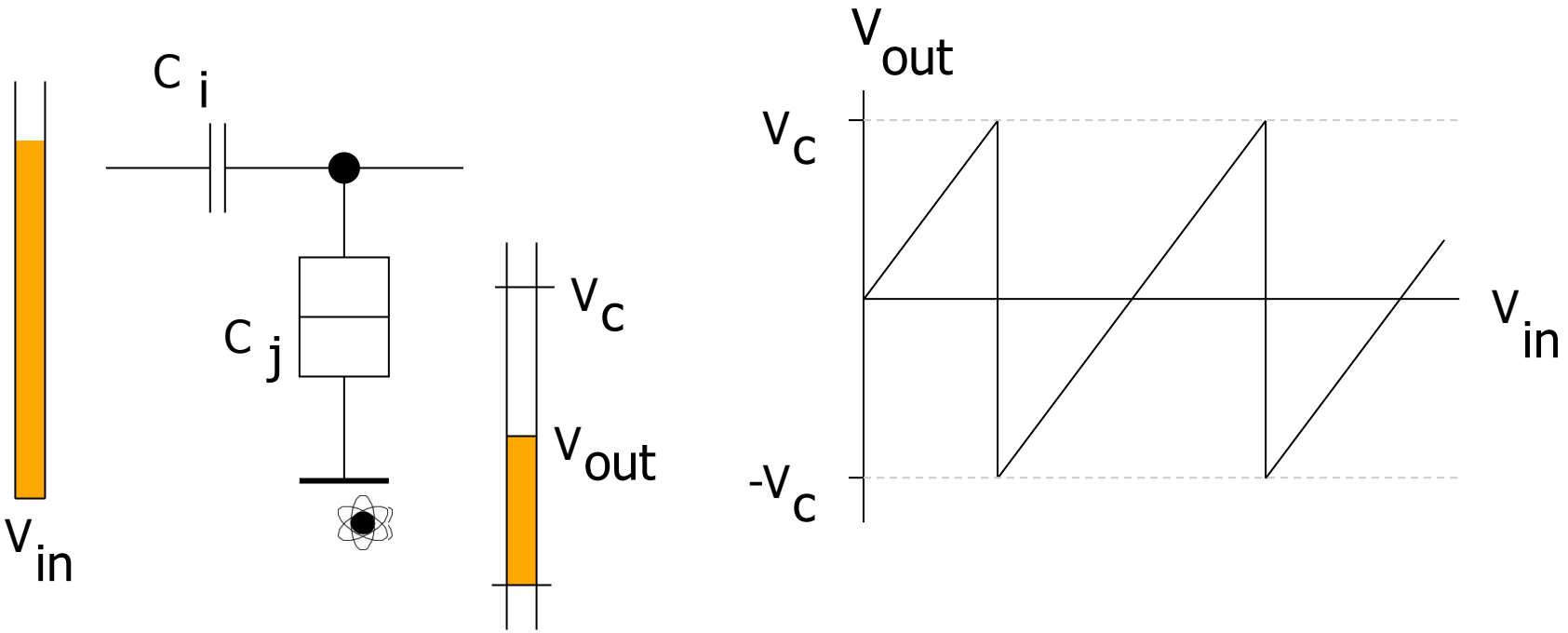
$$\Delta E = q_e(|V_j| - V_c)$$

Traditional Way

- Mimic the behavior of the MOS transistor
  - Delay:
    - O(100+) electrons tunnel per switching event
  - Power:
    - Large designs have leakage currents.

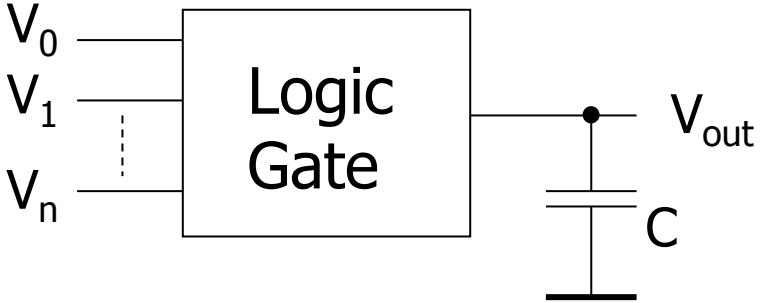


Electron Trap



- Can control the transport of individual electrons.
- Electrons are transported one at a time.
- The less transported, the faster the circuit!

Single Electron Encoded Logic



- Represent bits by single electrons
  - '0' = 0 electron
  - '1' = 1 electron
- Logic gate removes 1 electron from the output node if result is Boolean '1'.

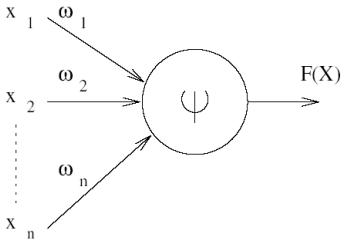
$$V_{out} = \frac{-q_e}{C} \qquad V_{out} = \frac{1.602e^{-19}(C)}{10e^{-18}(F)} = 16mV$$

Typically C is 10 aF.

- C. Lageweg, S. Cotofana, and S. Vassiliadis "A Linear Threshold Gate Implementation in Single Electron Technology", IEEE Computer Society Annual Workshop on VLSI (WVLSI2001), pp. 93-98, Orlando, Florida, USA, 2001.
- C. Lageweg, S. Cotofana, and S. Vassiliadis, "Single Electron Encoded Latches and Flip-Flops", IEEE Transactions on Nanotechnology, pp. 237-248, Vol. 3, No. 2, June 2004.

Threshold Logic

- An n-input linear Threshold Logic Gate (TLG) can compute any linearly separable Boolean function given by:



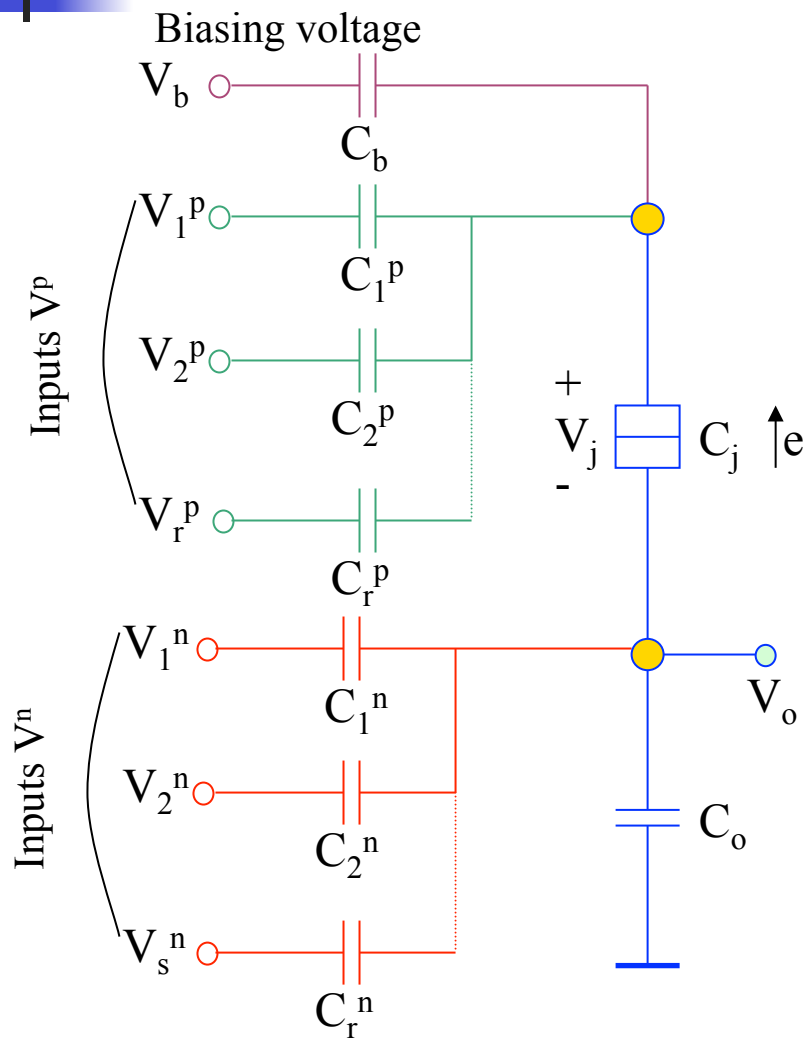
$$F(X) = sgn\{\mathcal{F}(X)\} = \begin{cases} 0 & \text{if } \mathcal{F}(X) < 0 \\ 1 & \text{if } \mathcal{F}(X) \geq 0 \end{cases}$$

$$\mathcal{F}(X) = \sum_{i=1}^{n} \omega_i x_i - \psi$$

- A single n-input TLG can compute an n-input AND, OR, NAND or NOR function as follows:

$$\begin{aligned} AND(a_1, a_2, \ldots, a_n) &= sgn\{a_1 + a_2 + \ldots + a_n - n\} \\ OR(a_1, a_2, \ldots, a_n) &= sgn\{a_1 + a_2 + \ldots + a_n - 1\} \\ NAND(a_1, a_2, \ldots, a_n) &= sgn\{-a_1 - a_2 - \ldots - a_n + n - 1\} \\ NOR(a_1, a_2, \ldots, a_n) &= sgn\{-a_1 - a_2 - \ldots - a_n\} \end{aligned}$$

SEEL Linear Threshold Gate



How to construct a threshold gate:

- Start with an electron box circuit.
- Bias V_j around V_c with bias voltage V_b.
- Inputs V^p add to V_j.
- Inputs V^n subtract from V_j.

Result

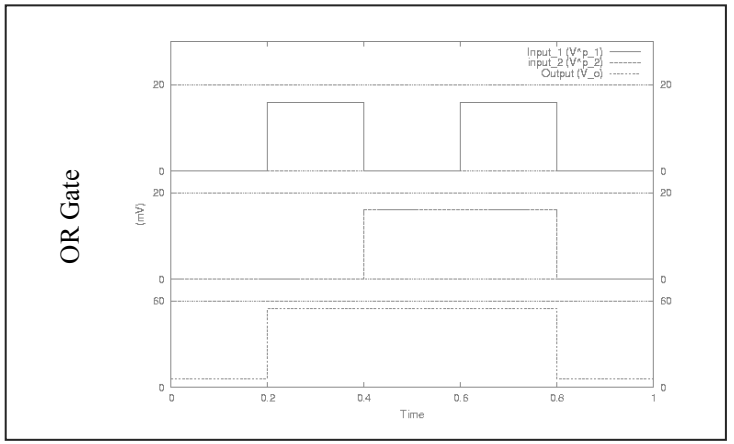
- When $V_j > V_c$ the output is 'high'.
- V_b act as threshold adjuster.

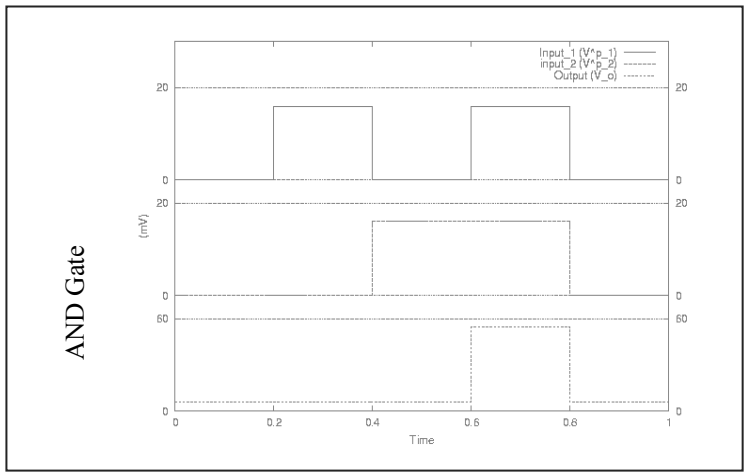
Formally

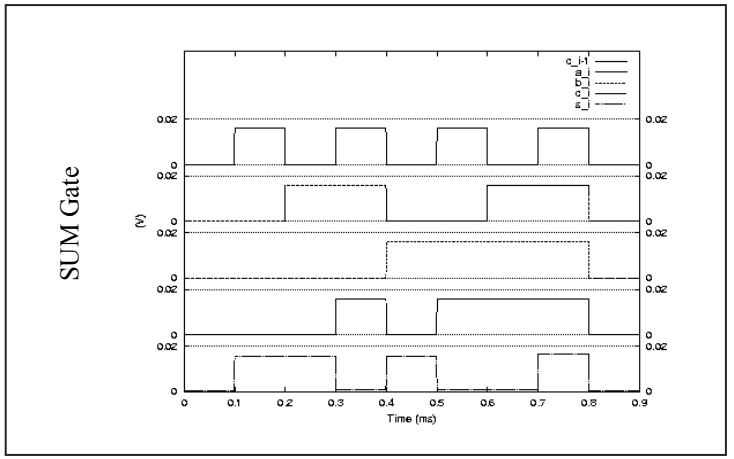
$$C_\Sigma^p = \Sigma C_l^p + C_b$$
$$C_\Sigma^n = \Sigma C_m^n + C_o$$
$$V_o = \mathrm{sgn}\{V_j - V_c\} = \mathrm{sgn}\{f(X)\}$$
$$f(X) = C_\Sigma^n \Sigma V_l^p C_l^p - C_\Sigma^p \Sigma V_m^n C_m^n - \Psi$$
$$\Psi = 0.5 (C_\Sigma^p + C_\Sigma^n) e - C_\Sigma^n C_b V_b$$

SEEL Threshold Gates

- AND gate
  a AND b = SGN {a + b - 2}
- OR gate
  a OR b = SGN{a + b - 1}
- Full Adder SUM gate
  S_i = sgn{$a_i + b_i + c_{i+1} - 2\,c_i - 1$}

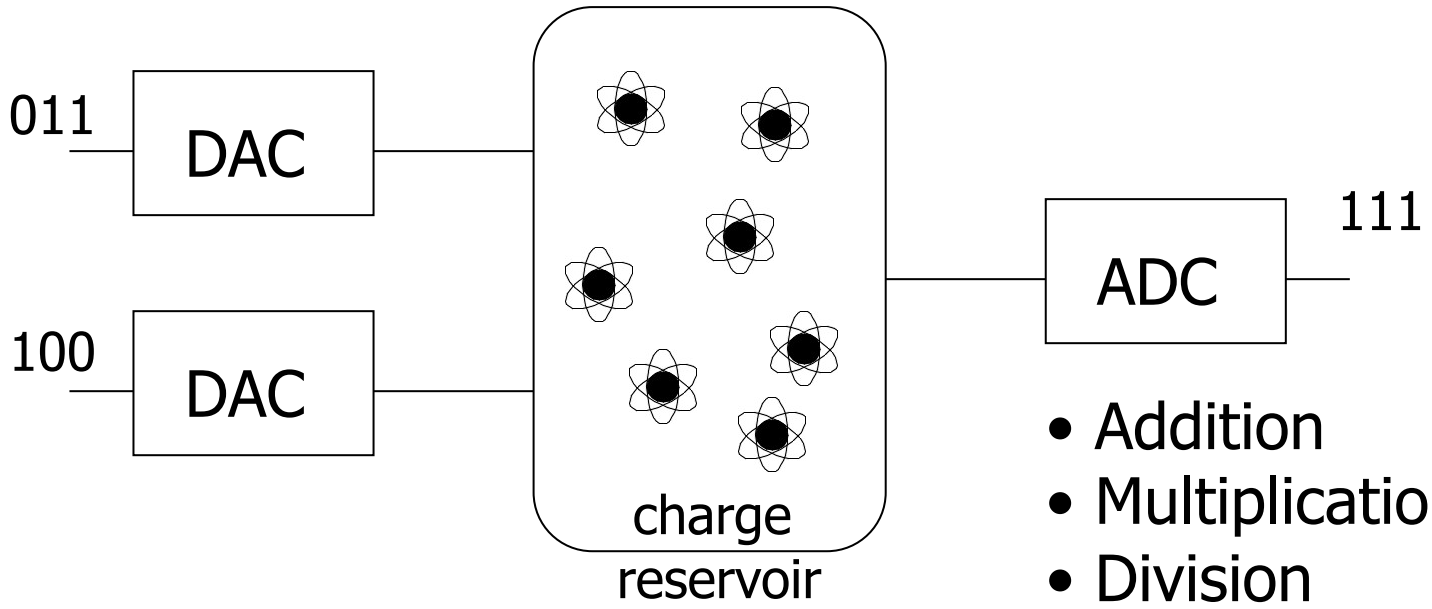






Electron Counting Paradigm

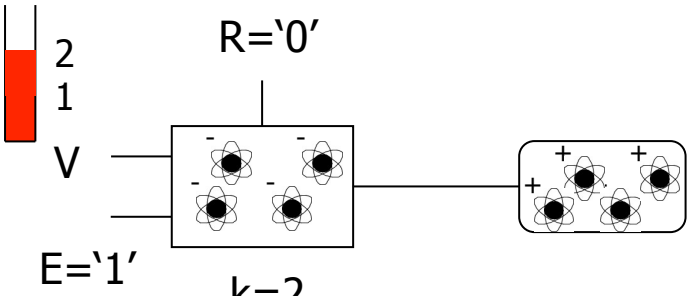
Basic Principle: Represent values by number of electrons.

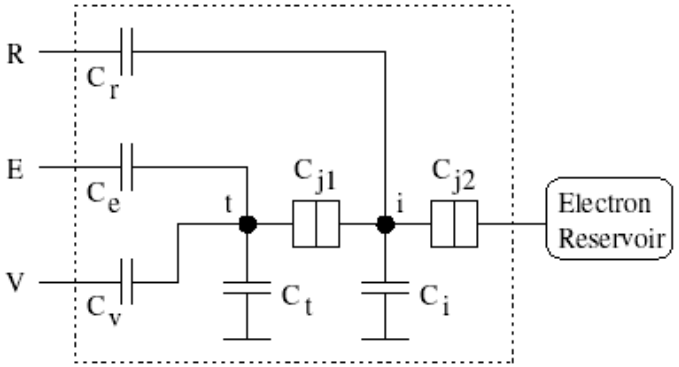


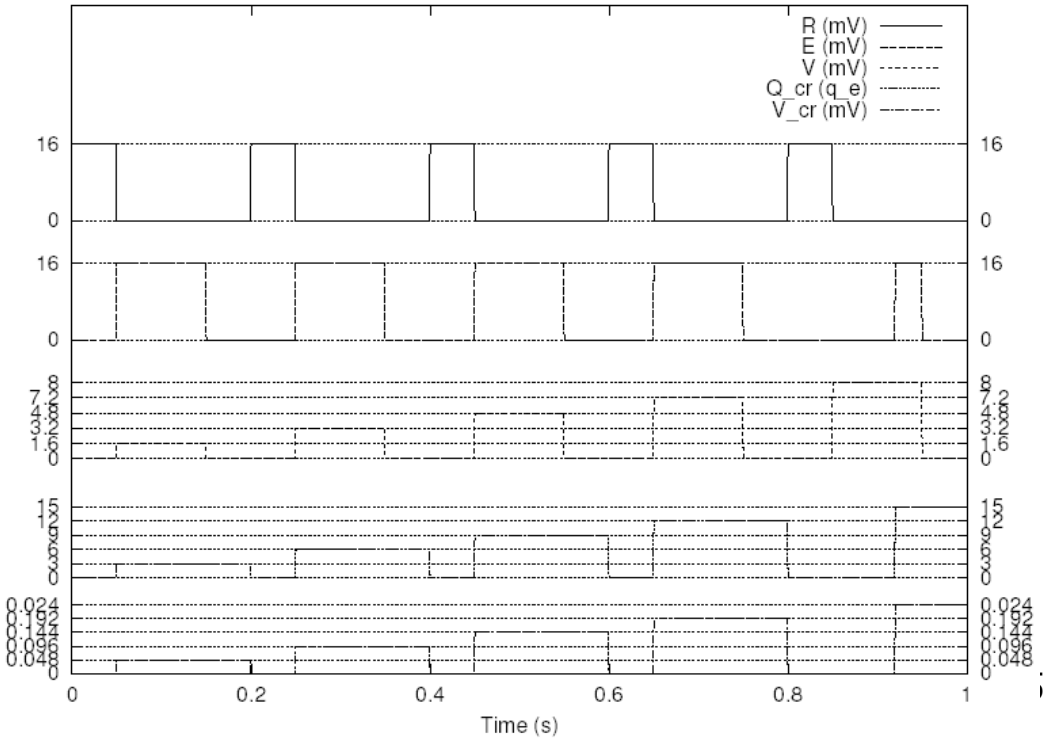
- C. Hu, S. Cotofana, and J. Jiang, "Digital-to-Analog Converter Based on Single-Electron Tunneling Transistors", IEE Proceedings Circuits, Devices & Systems, pp. 438-442, Vol. 151, No. 5, October 2004.
- C. Hu, S. Cotofana, J. Jiang, and Q. Cai, "Analog-to-Digital Converter Based on Single-Electron Tunneling Transistors", IEEE Transactions on VLSI Systems, pp. 1209-1213, Vol. 12, No. 11, November 2004.
- S. Cotofana, C. Lageweg, and S. Vassiliadis, "Addition Related Arithmetic Operations via Controlled Transport of Charge", IEEE Transaction on Computers, Vol. 54, No. 3, pp. 243-256, March 2005.
- C.H. Meenderinck, S. Cotofana, "Computing Division using Single Electron Tunneling Technology", IEEE Transactions on Nanotechnology, pp. 451-459, Vol. 6, No. 4, July 2007.

Move k electron (MVke) Block

When enabled (re)moves V*k electrons (from) to a reservoir.

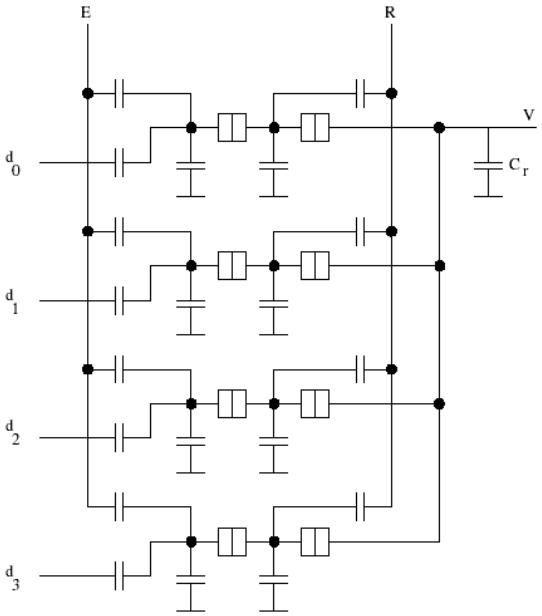


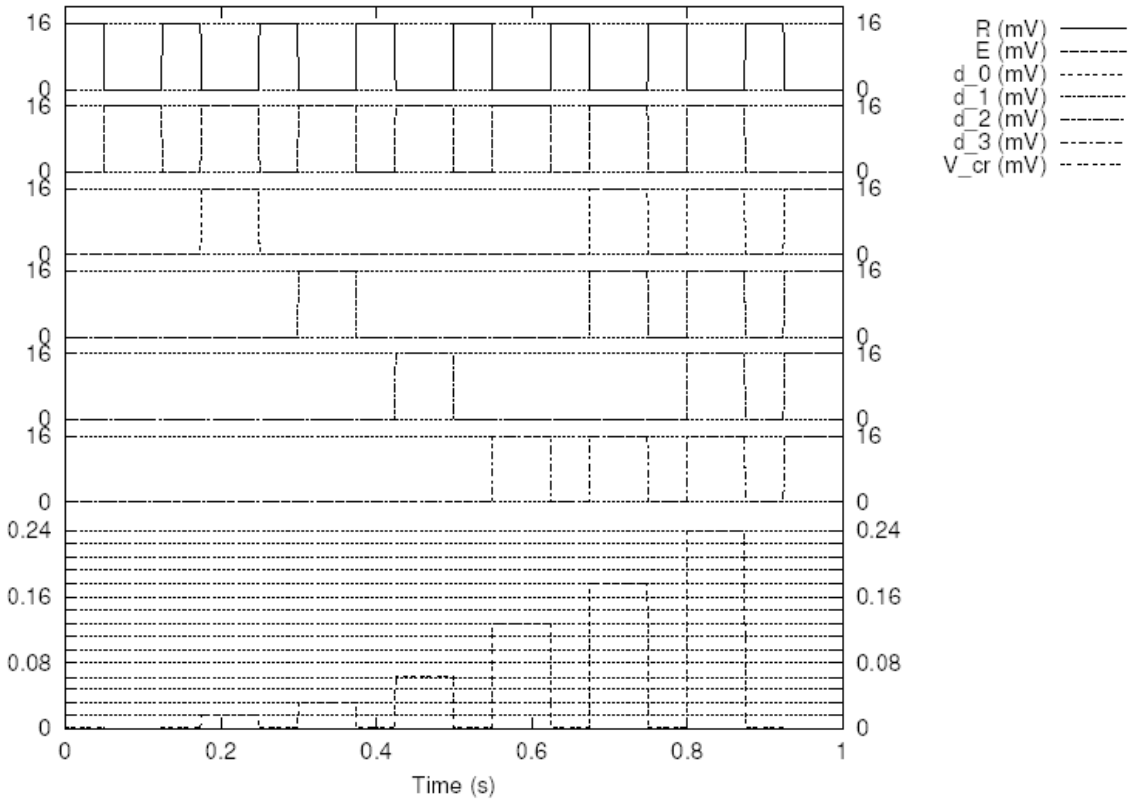




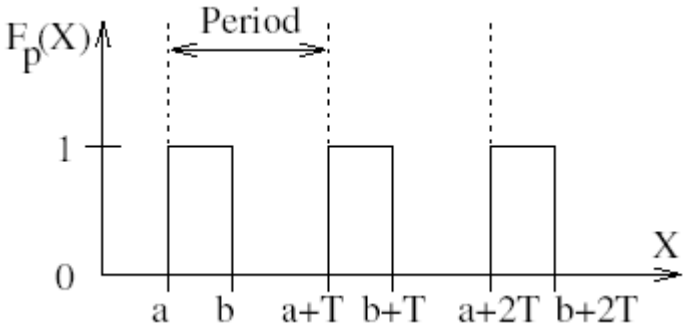
4-bit Digital to Analog Converter

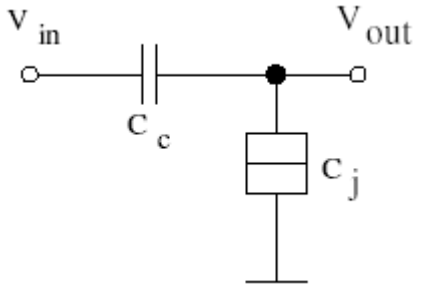
- Requires 4 Mvke blocks.



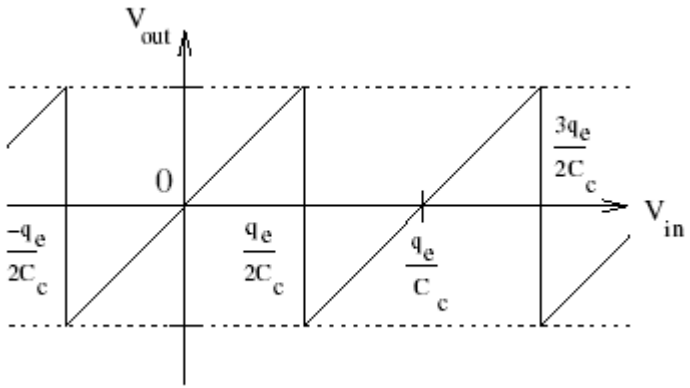


Periodic Symmetric Function



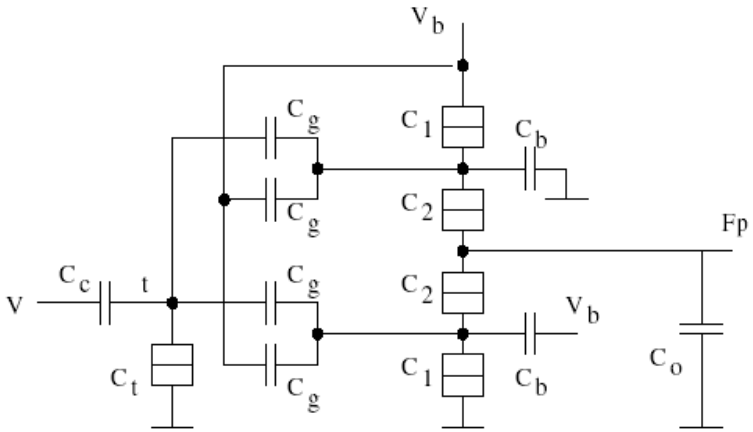


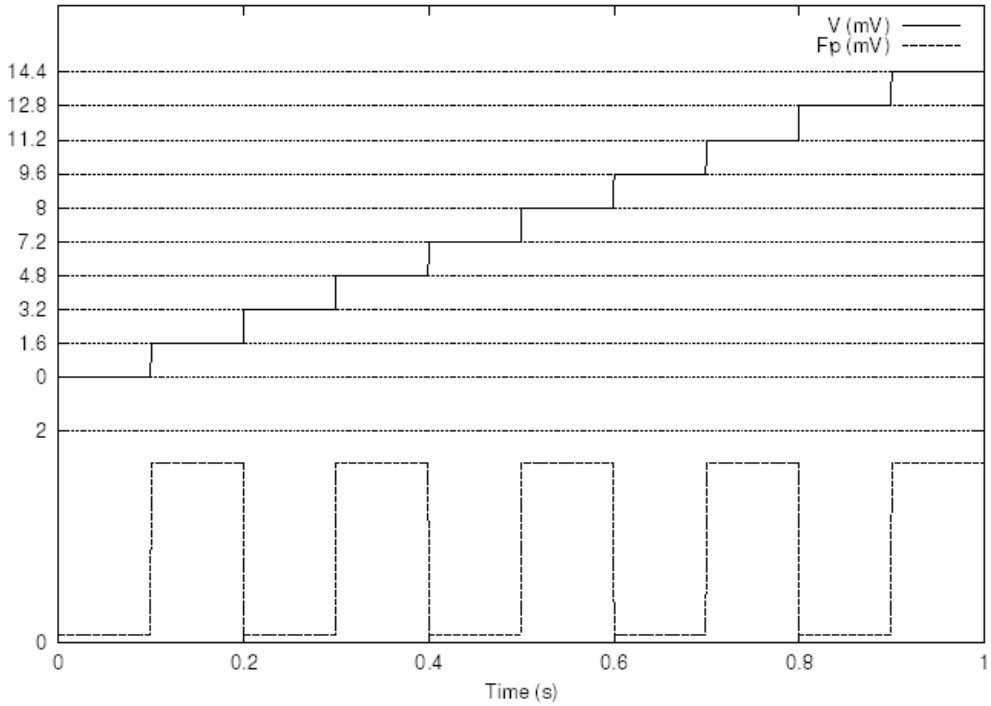
- Can evaluate a PSF function characterized by a, b, and T.
- PSF functions important for many arithmetic functions such as parity and counting.
- The electron trap circuit displays periodic behavior.



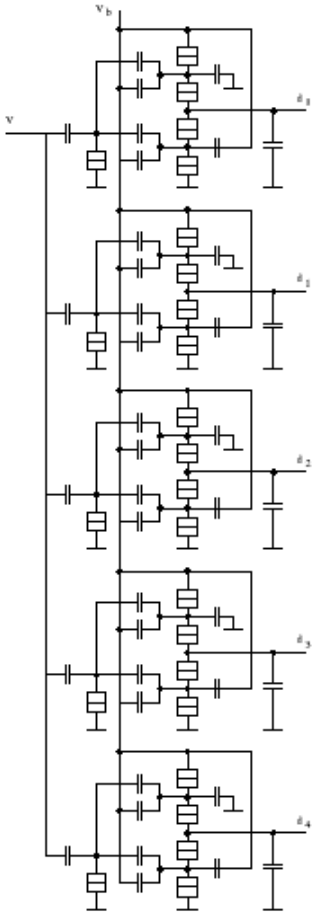
PSF Block Implementation

- A SET inverter is used to implement a literal function such that
  - F_p = '0' if V_{out} (trap) > 0
  - F_p = '1' if V_{out} (trap) < 0

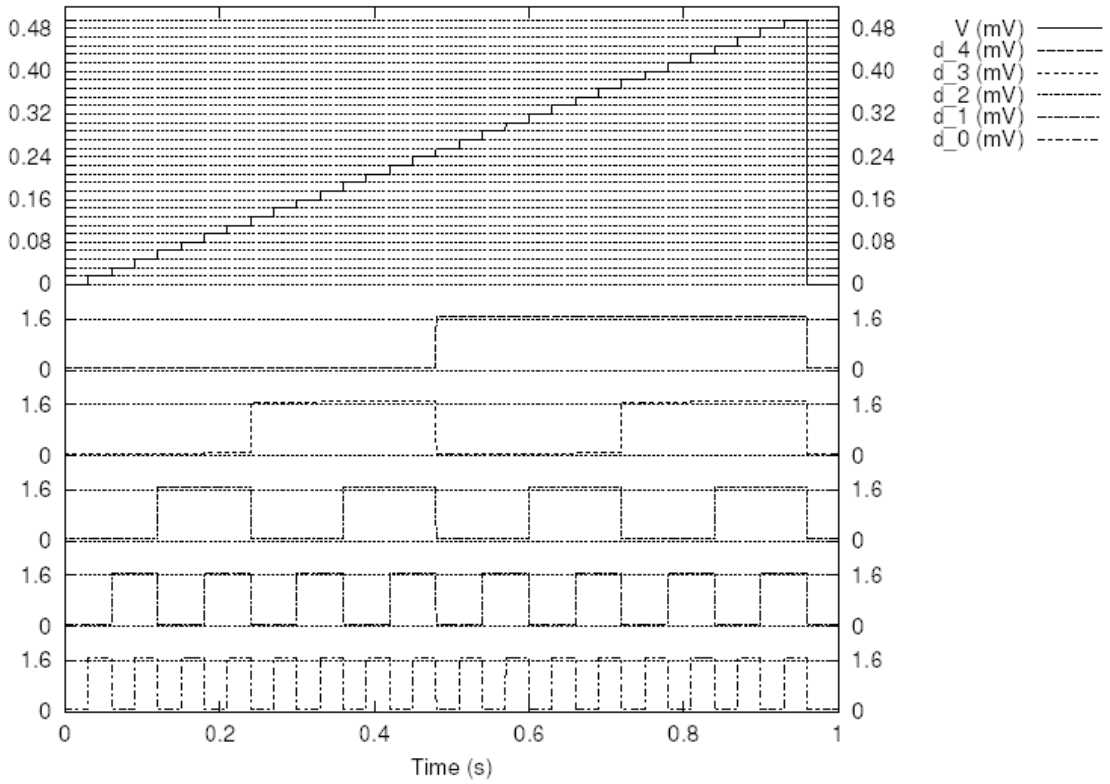




5-bit Analog to Digital Converter

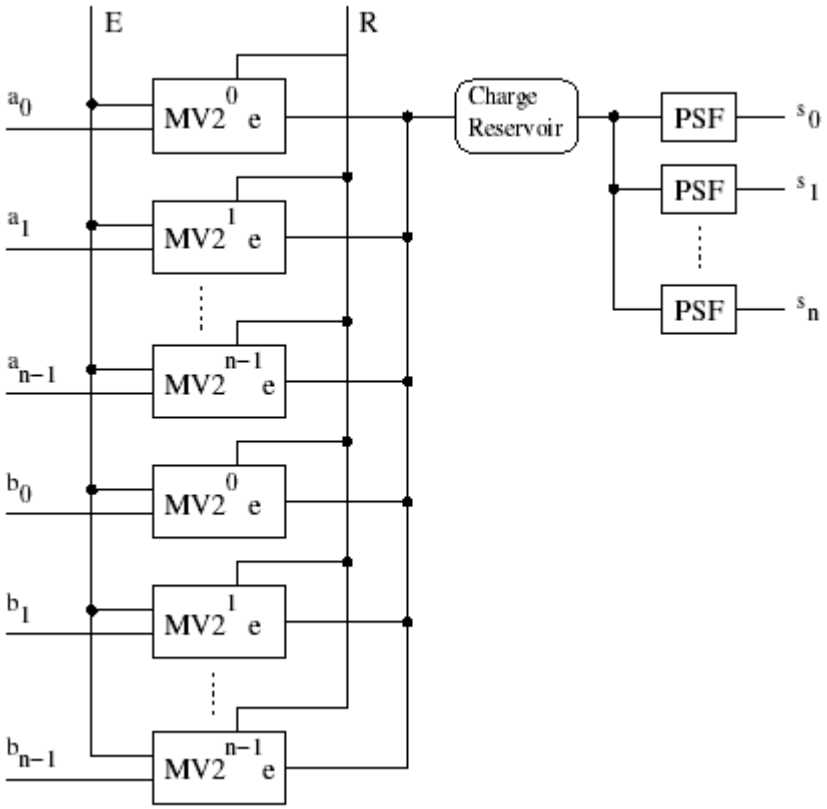


- Requires 5 PSF blocks.



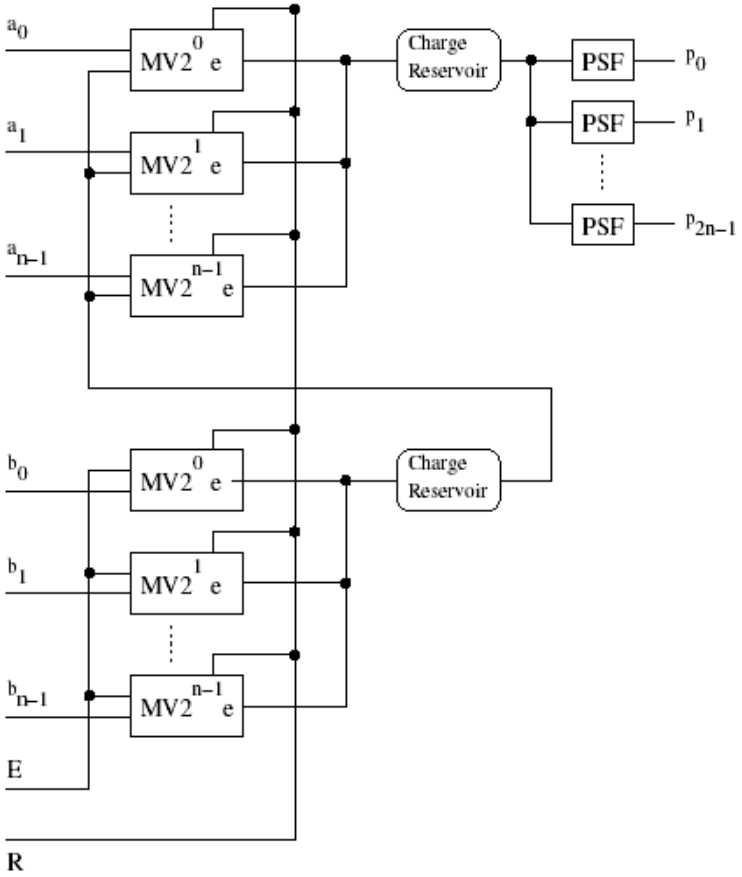
Electron Counting Addition

- A and B are converted to the charge encoded representation.
- By utilizing a common charge reservoir for A and B the addition operation is implemented at no additional costs.
- The charge encoded representation of A+B is reconverted to binary by n+1 PSF blocks.
- Adding two n-bit operands requires a depth-2 network composed of 3n +1 EC components (Mvke and PSF block).
- The addition scheme can be utilized to implement parity, multi-operand addition and n/log n counting functions.



Electron Counting Multiplication

- B is converted to the charge encoded representation.
- The charge encoded value B serves as input V, the input bits a_i are used as enable (E) signals.
- The charge encoded representation of A·B is reconverted to binary by n+1 PSF blocks.
- Multiplying two n-bit operands requires a depth-3 composed of 4n EC components.



How to Deal with Noise and Fluctuations?

Is Noise our Real Enemy?

Noise and Fluctuations

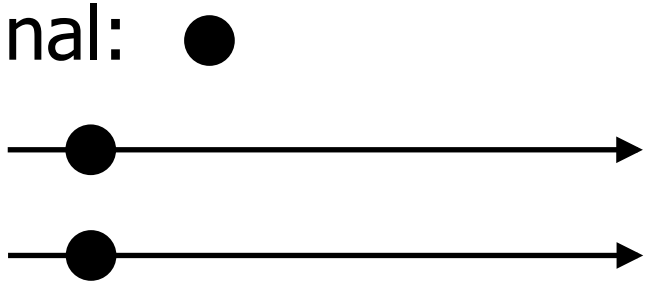
- Suppress: Difficult when signal level approaches noise level.

- Use Redundancy: Error Correcting Codes (ECC)

- Accept and Exploit: Use unconventional methods, e.g.,
  - encoding signals by independent noise sources,
  - enhancing signals through stochastic resonance, and
  - synchronizing elements in a distributed systems by common noise.

Signal Representation

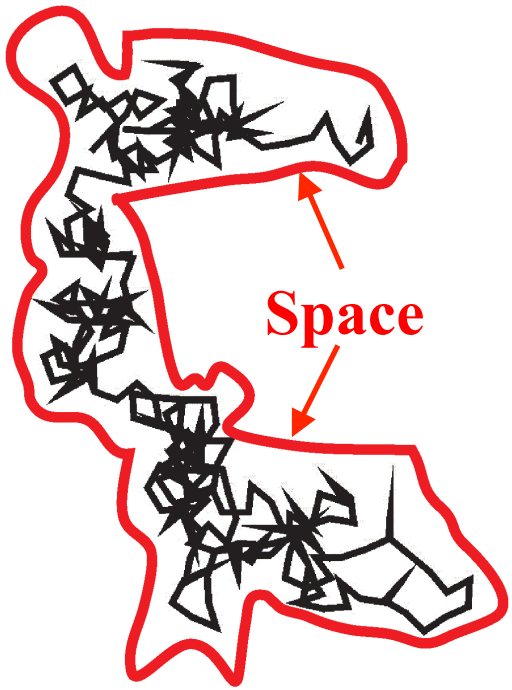
- Less carriers to represent signal:
- Token-based circuits:
- Noise and Fluctuations:



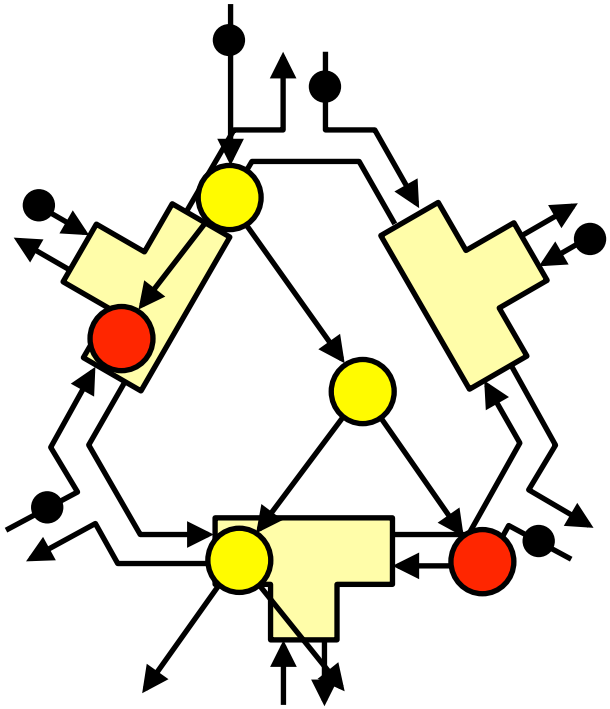
Our Approach

- No clock: wires more local, less heat dissipation
- Delay-insensitive circuits: robust to signal delays
- Brownian motion of signals: allow... and, exploit

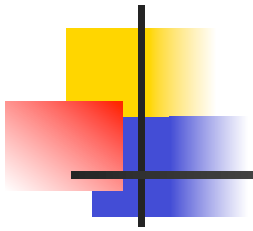
How to Exploit Noise?



Search in space through Brownian Motion



Similarly, circuit state space can be searched

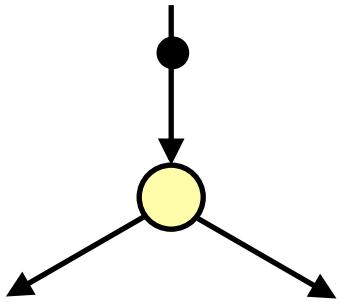


Use Fluctuations for Stochastic Search

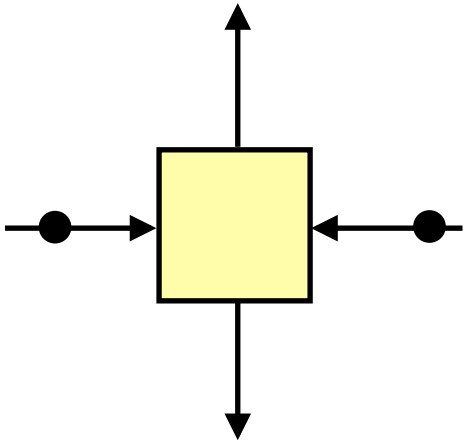
- Conducting random walk in a (state) space to find one optimal or sub-optimal state.
- Usually driven by Brownian motion.
- In nature it brings together agents so that they can react with each other.
- Fluctuations act like a substitute for a control mechanism.

Brownian Circuits

Universal set of circuit primitives



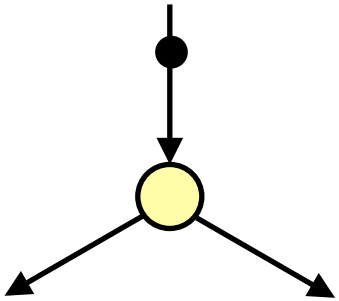
Hub



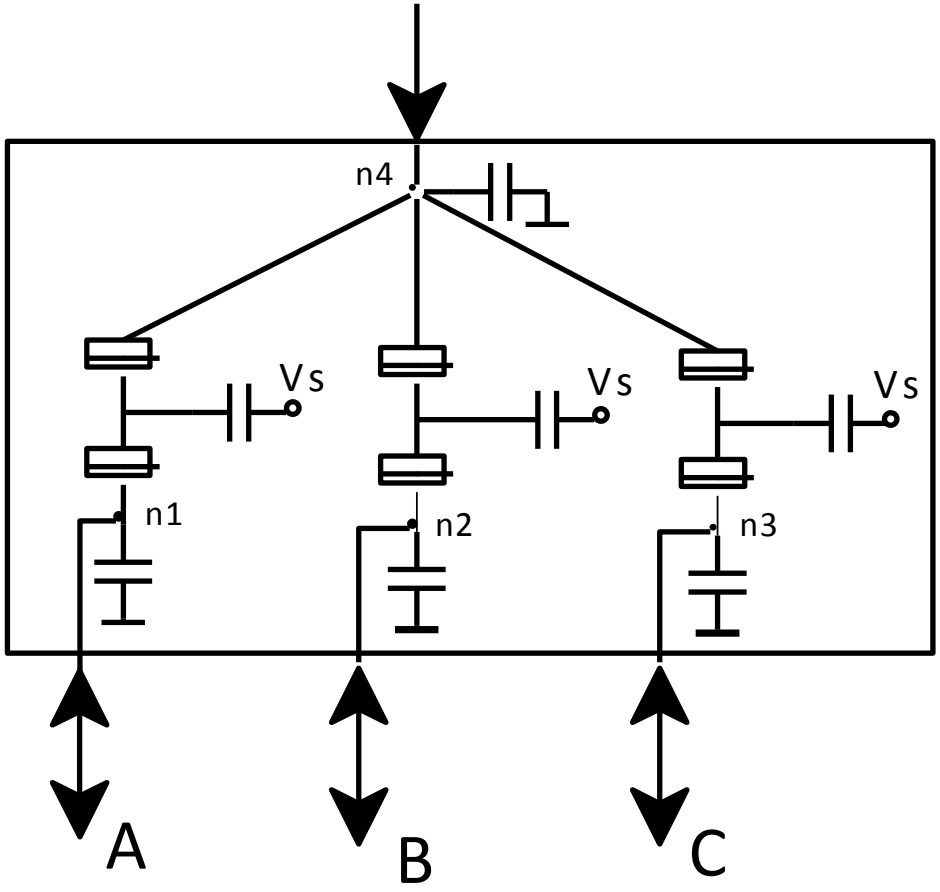
CJoin

- S. Safiruddin, S.D. Cotofana, F. Peper, and J. Lee, "Building Blocks for Fluctuation Based Calculation in Single Electron Tunnelling Technology", 8th IEEE International Conference on Nanotechnology, Arlington, Texas, USA, August 2008.
- S. Safiruddin, S. D. Cotofana, and F. Peper "Stigmergic Search with Single Electron Tunneling Technology Based Memory Enhanced Hubs", 2012 ACM/IEEE International Symposium on Nanoscale Architectures, pp. 110 - 115, Amsterdam, The Netherlands, July 2012.

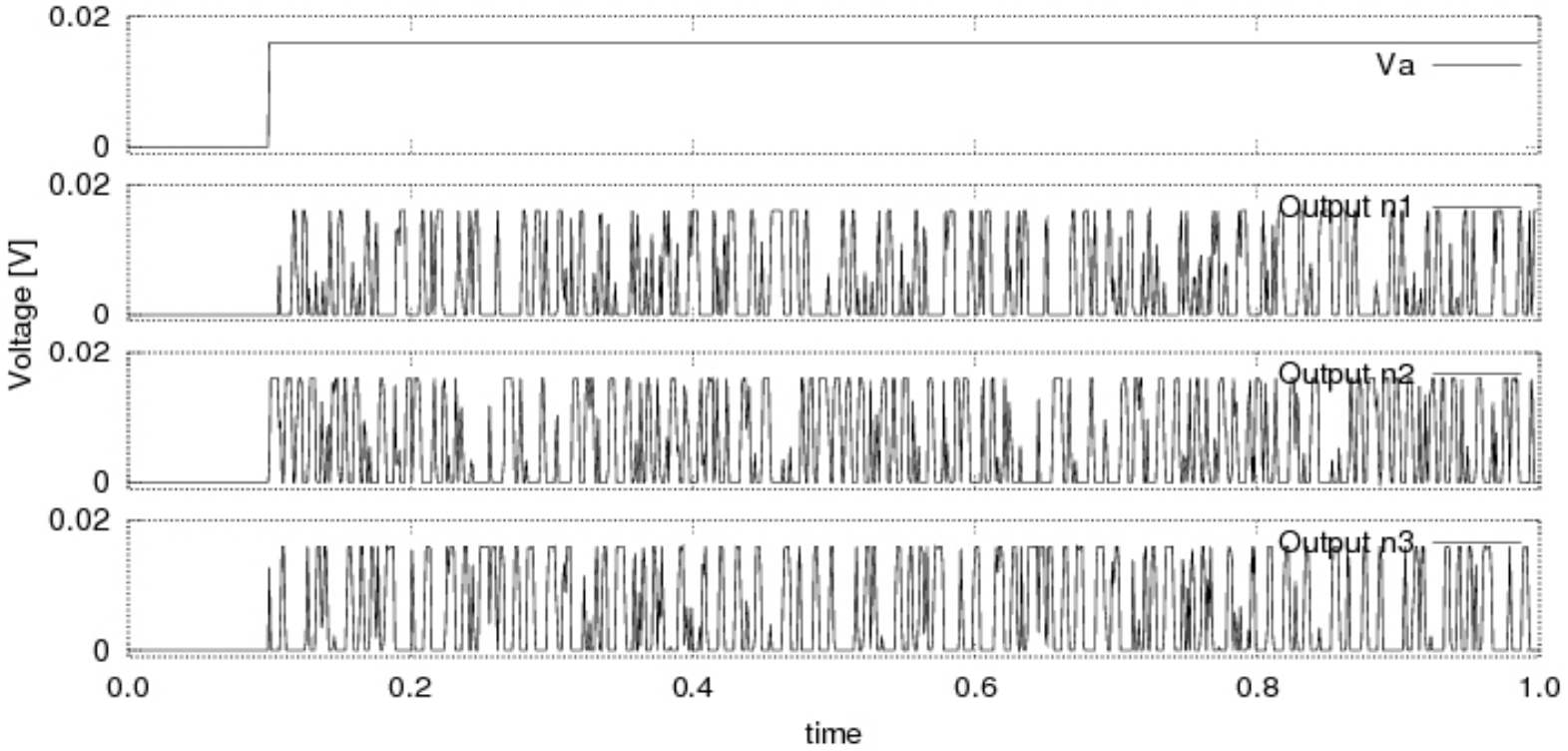
Hub



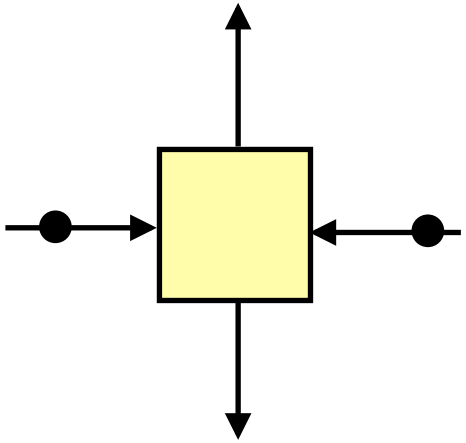
Hub



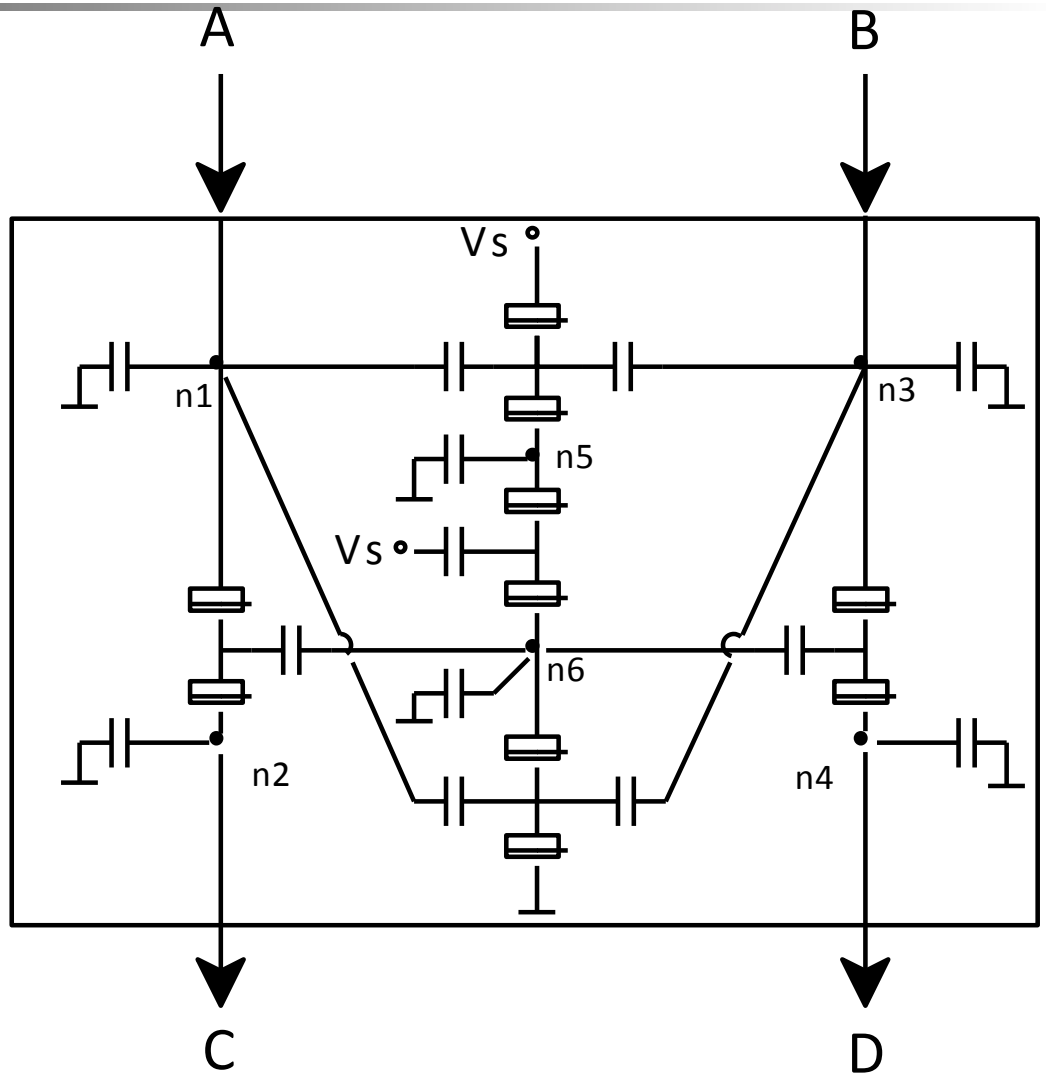
Hub Simulation



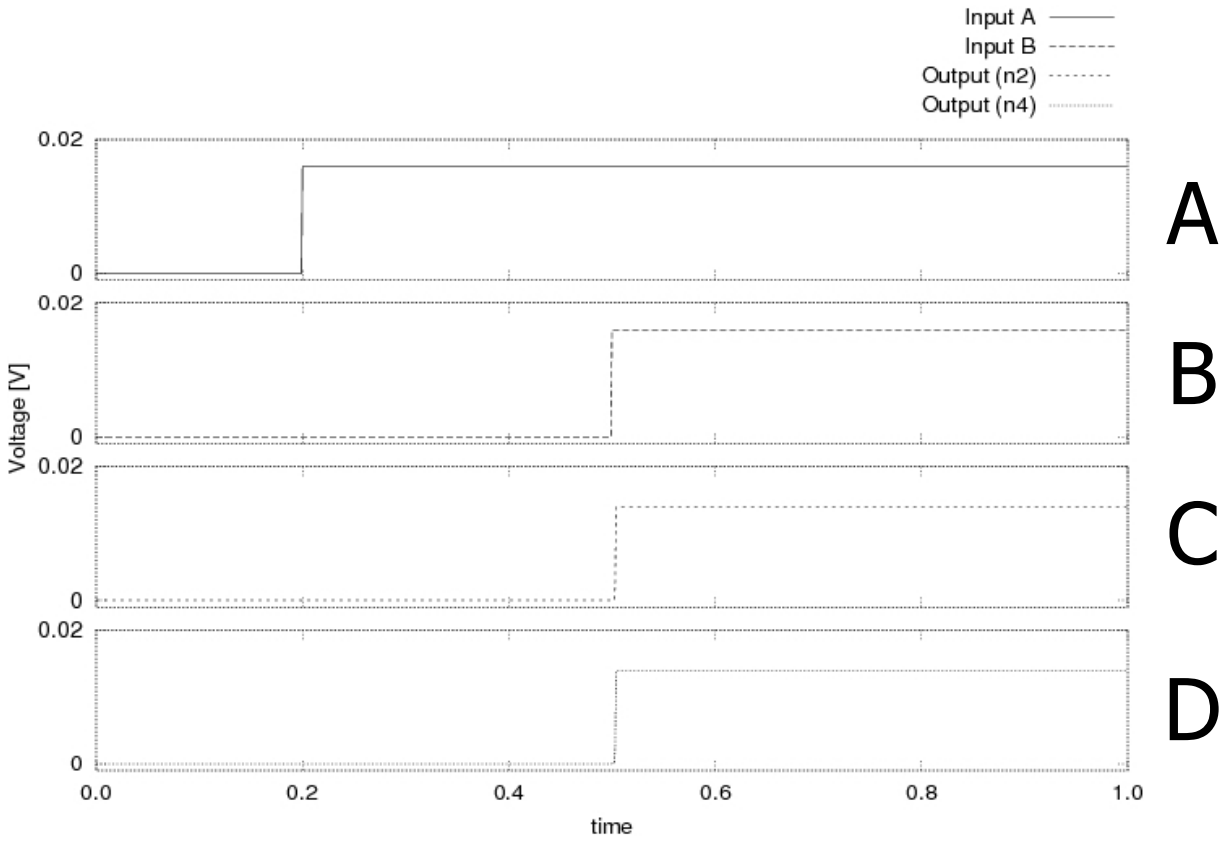
Conservative Join



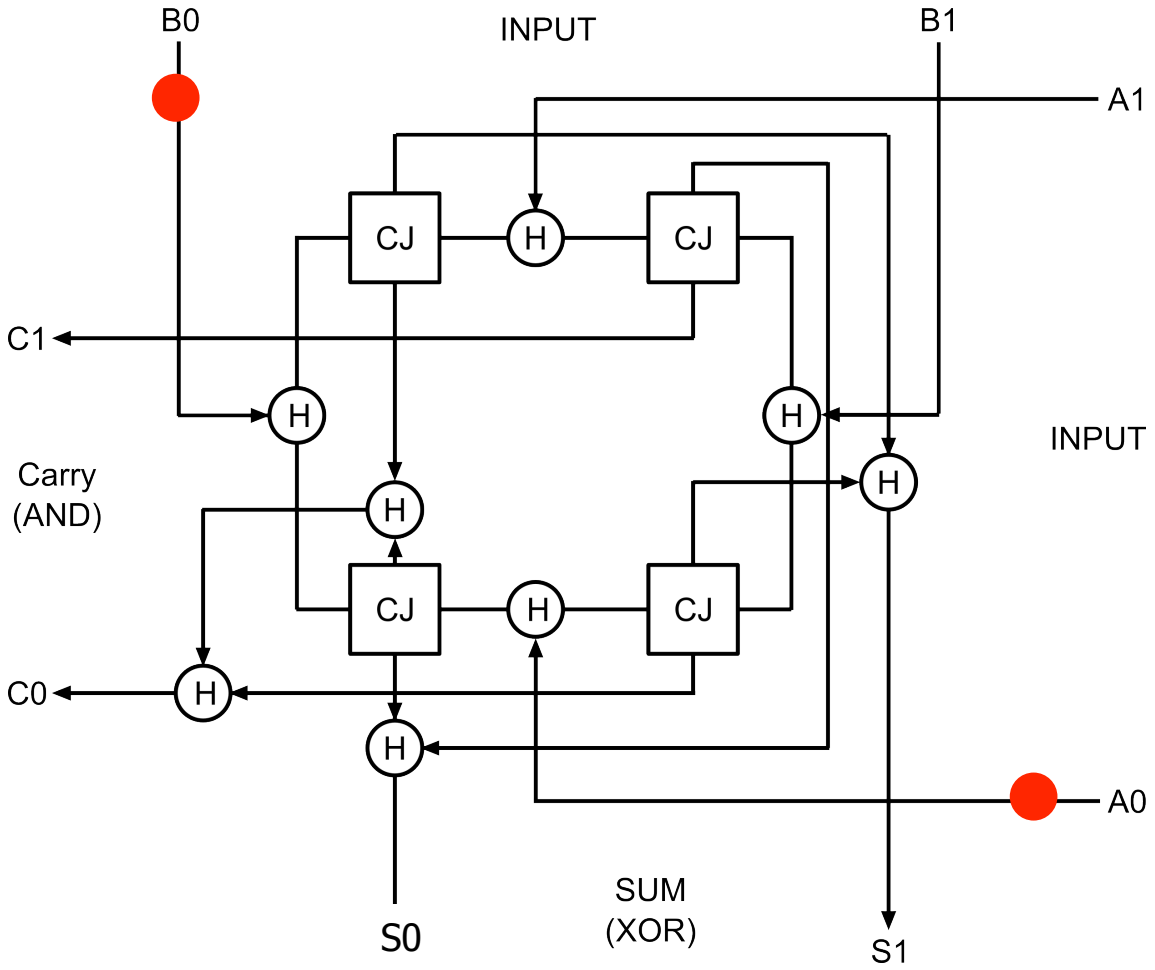
CJoin



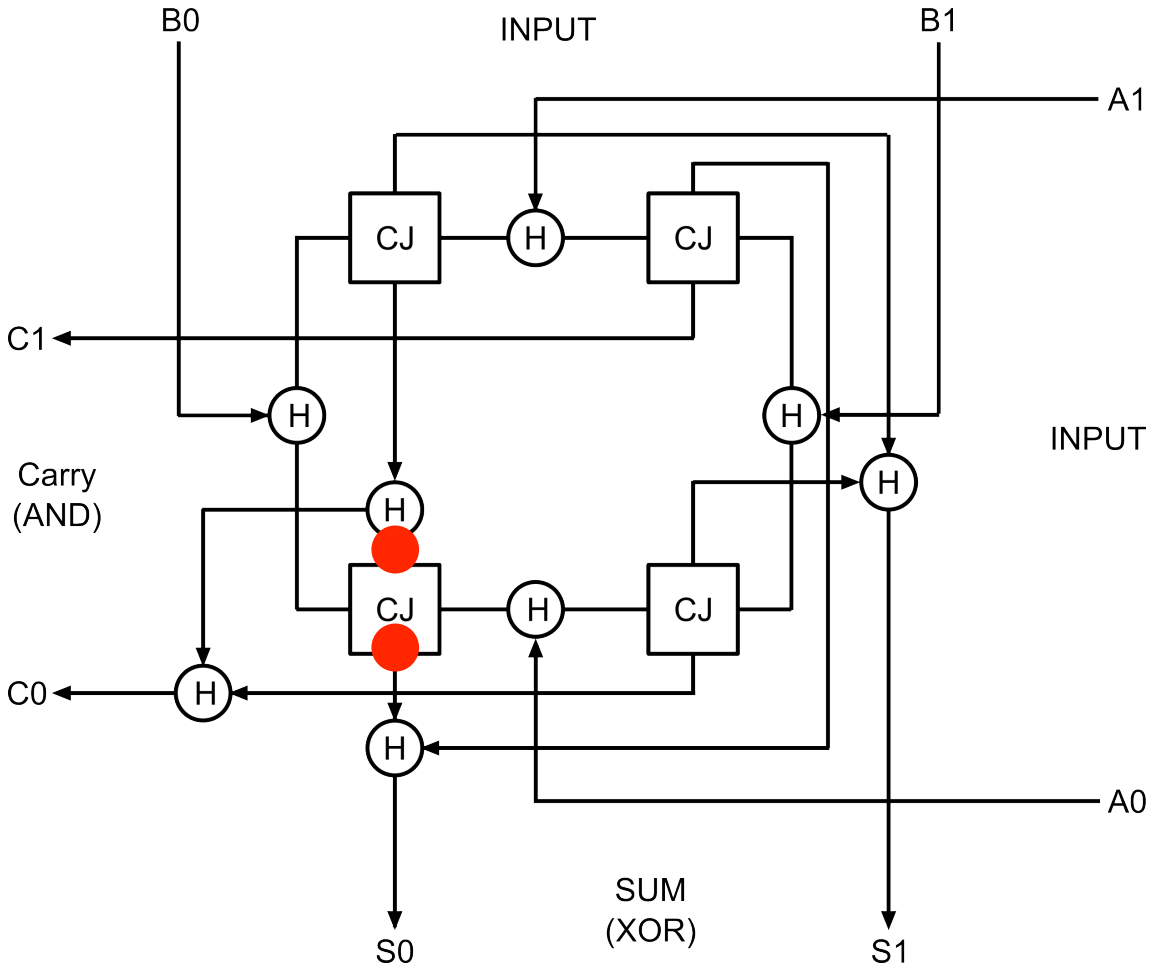
CJ Simulation



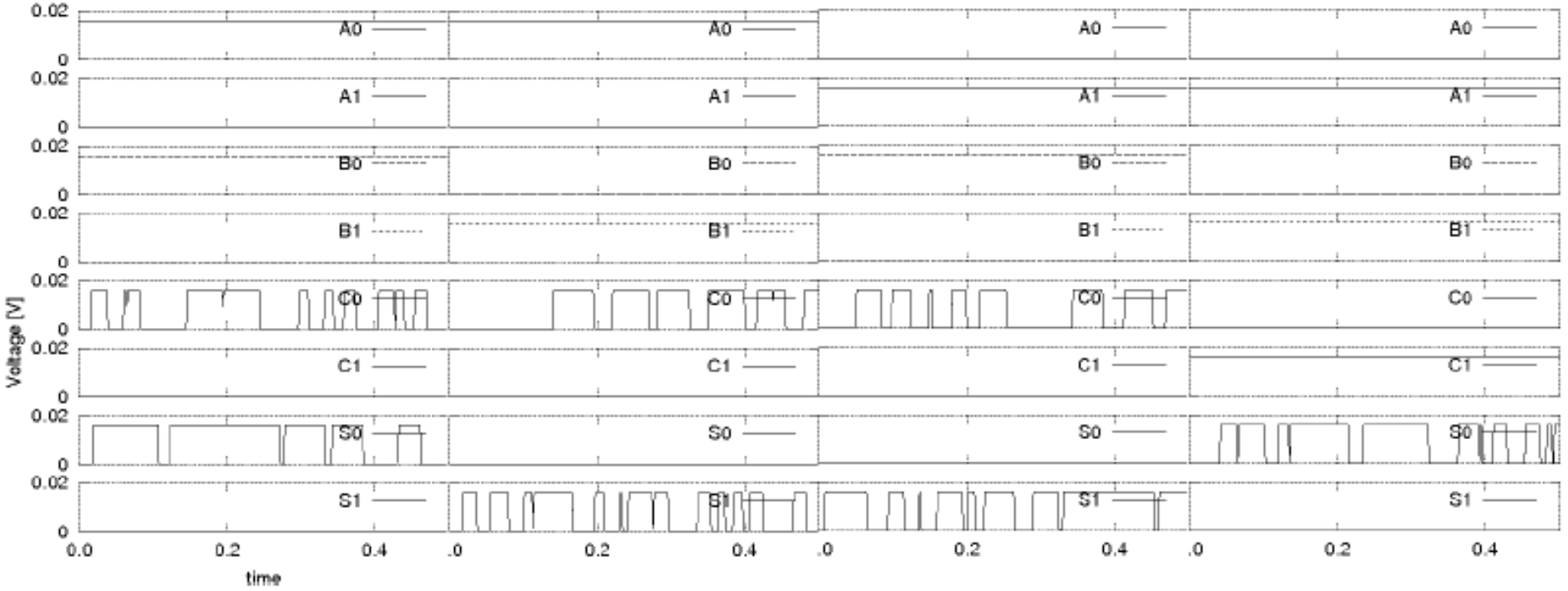
Half-Adder


B0
INPUT
B1
A1
CJ
H
CJ
C1
H
H
INPUT
Carry
(AND)
H
H
CJ
H
CJ
C0
H
H
A0
SUM
(XOR)
S0
S1

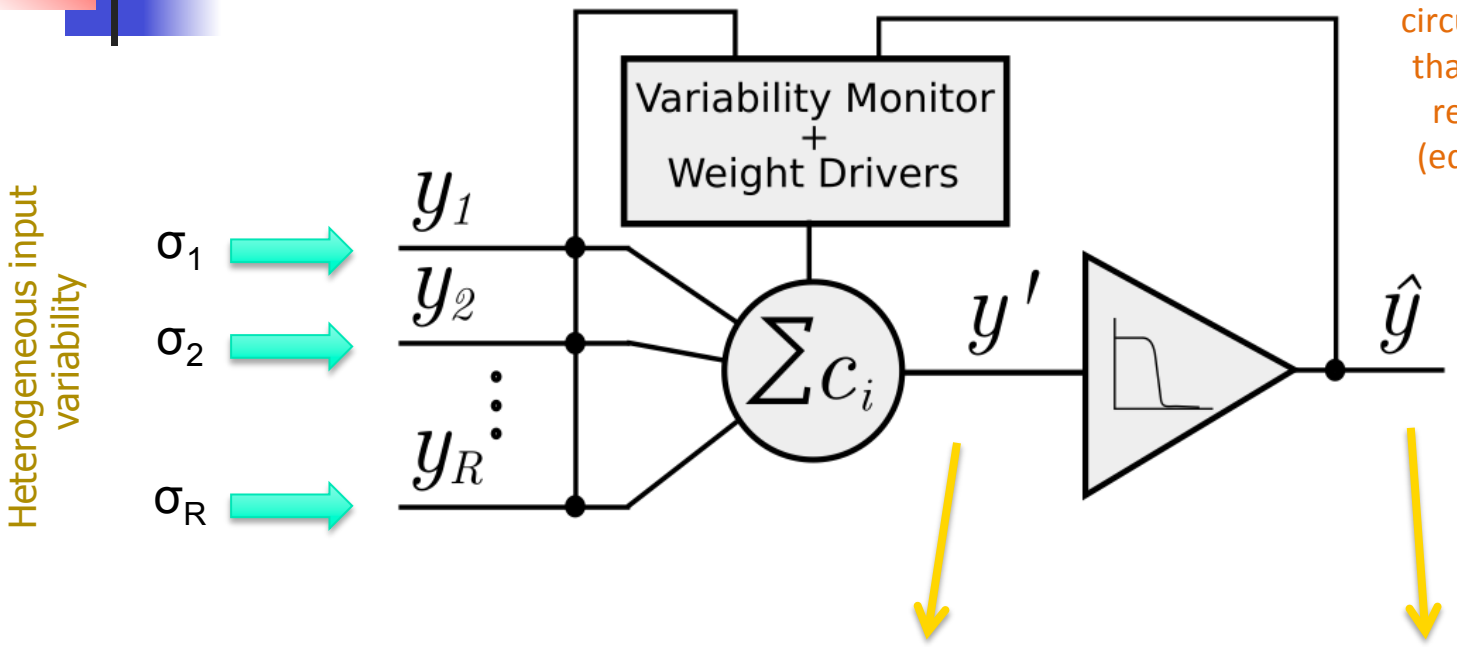
Half-Adder


B0
INPUT
B1
A1
CJ
H
CJ
C1
H
H
INPUT
Carry
(AND)
H
H
CJ
H
CJ
C0
H
H
A0
SUM
(XOR)
S0
S1

Half-adder Simulation



Adaptive Averaging Cell (AD-AVG)



AD-AVG YIELD = % of circuits in a MC simulation that satisfy the reliability requirement Pe < 10^{-4} (equivalently $\sigma_{y'} < \sigma_{max}$ = 0.1344 V).

R input replicas:

$$y_i = y + \eta_i$$
$$\eta_i \sim N(0, \sigma_i)$$

$$\sigma_{y'} = \sqrt{\sum_{i=1}^{R} c_i^2 \sigma_i^2}$$

$$P_e = \frac{1}{2} \times \mathrm{erfc}\left(\frac{V_{cc}}{\sqrt{8}\sigma_{y'}}\right)$$

- A. Nivard, S. D. Cotofana, A. Rubio, "Adaptive Fault-Tolerant Architecture for Unreliable Device Technologies", 11th IEEE Conference on Nanotechnology, Portland, Oregon, USA, August 2011.
- N. Aymerich, S. D. Cotofana, and A. Rubio, "Adaptive Fault-Tolerant Architecture for Unreliable Technologies with Heterogeneous Variability", IEEE Transactions on Nanotechnology, pp. 818-829, Vol. 11, No.4, July 2012.

Degradation Stochastic Resonance (DSR)

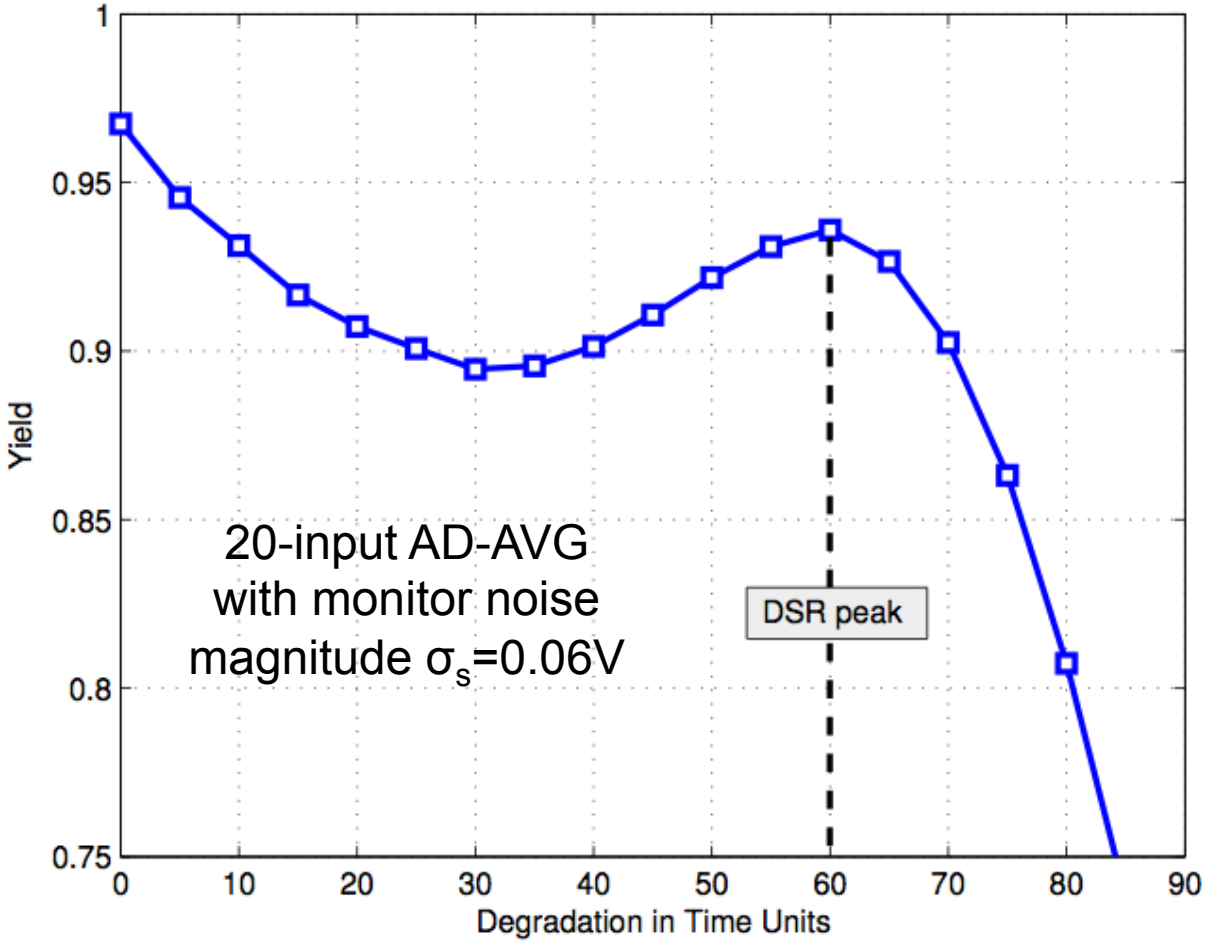
Optimum weights

$$c_i^{opt} = \frac{\sigma^2_{y'\ \min}}{\sigma_i^2}$$

Imperfect variability monitor

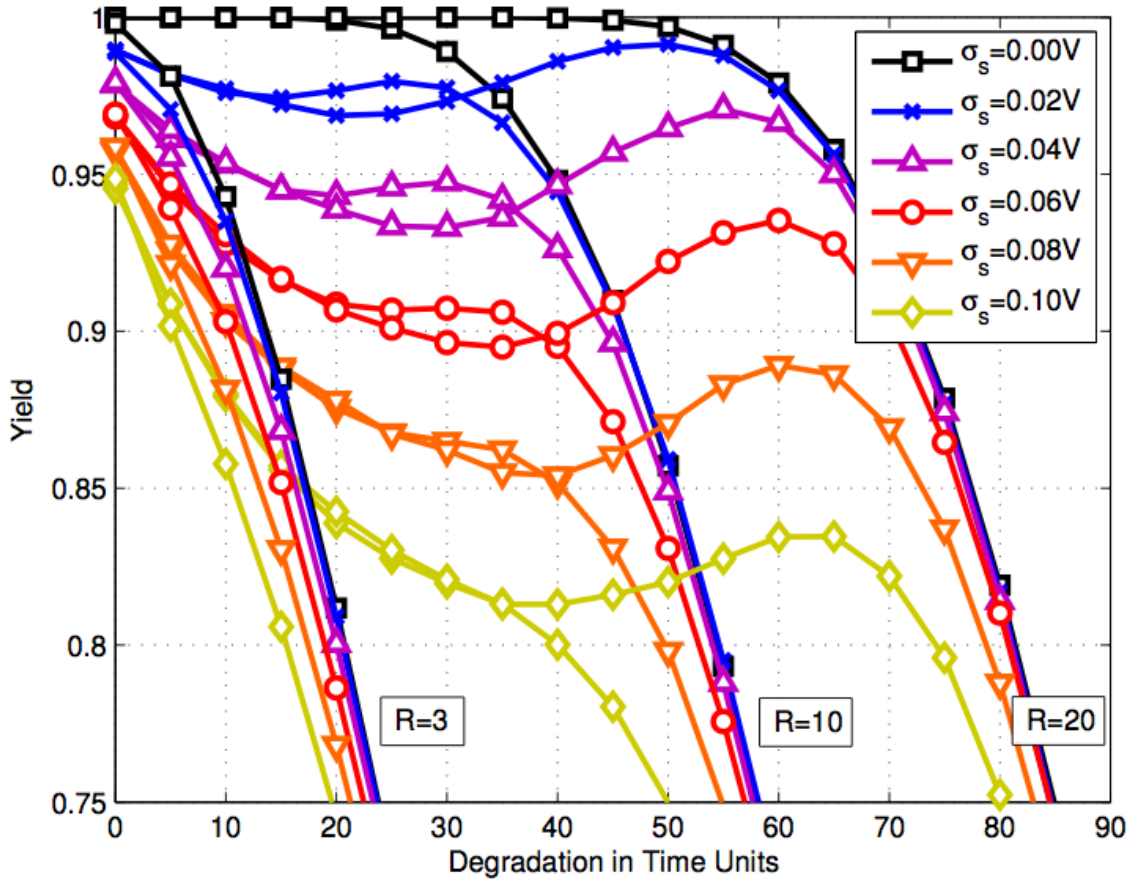
$$\widehat{\sigma_i^2} = \sigma_i^2 + \xi_i$$

$$\xi_i \sim N(0, \sigma_s)$$

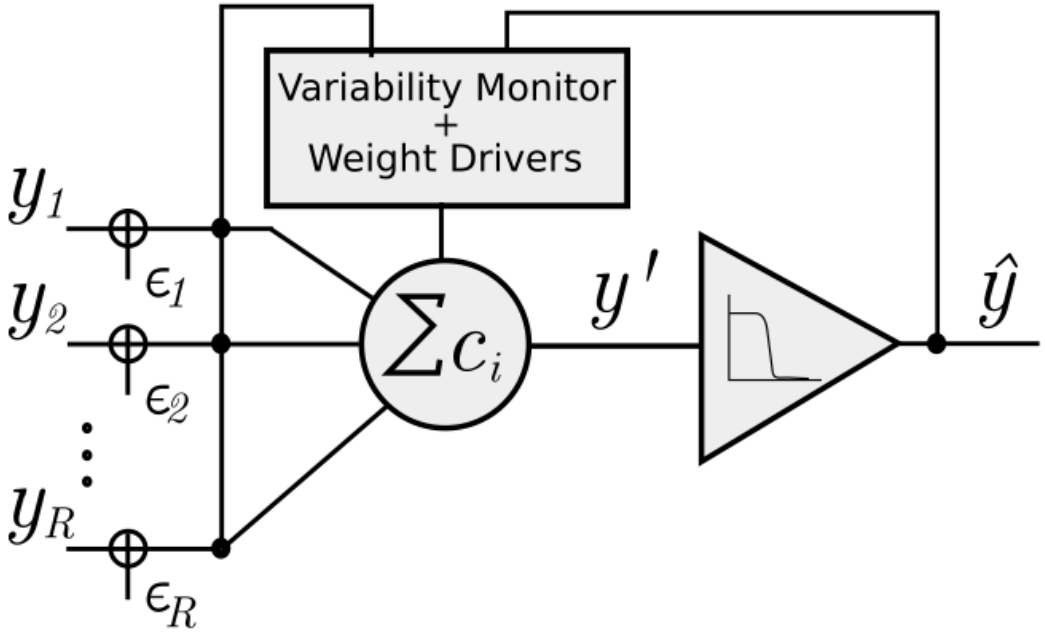


- N. Aymerich, S.D. Cotofana, A. Rubio, "Degradation Stochastic Resonance (DSR) in AD-AVG Architectures", 12th IEEE Conference on Nanotechnology, Birmingham, UK, August 2012,

Degradation Stochastic Resonance (DSR)



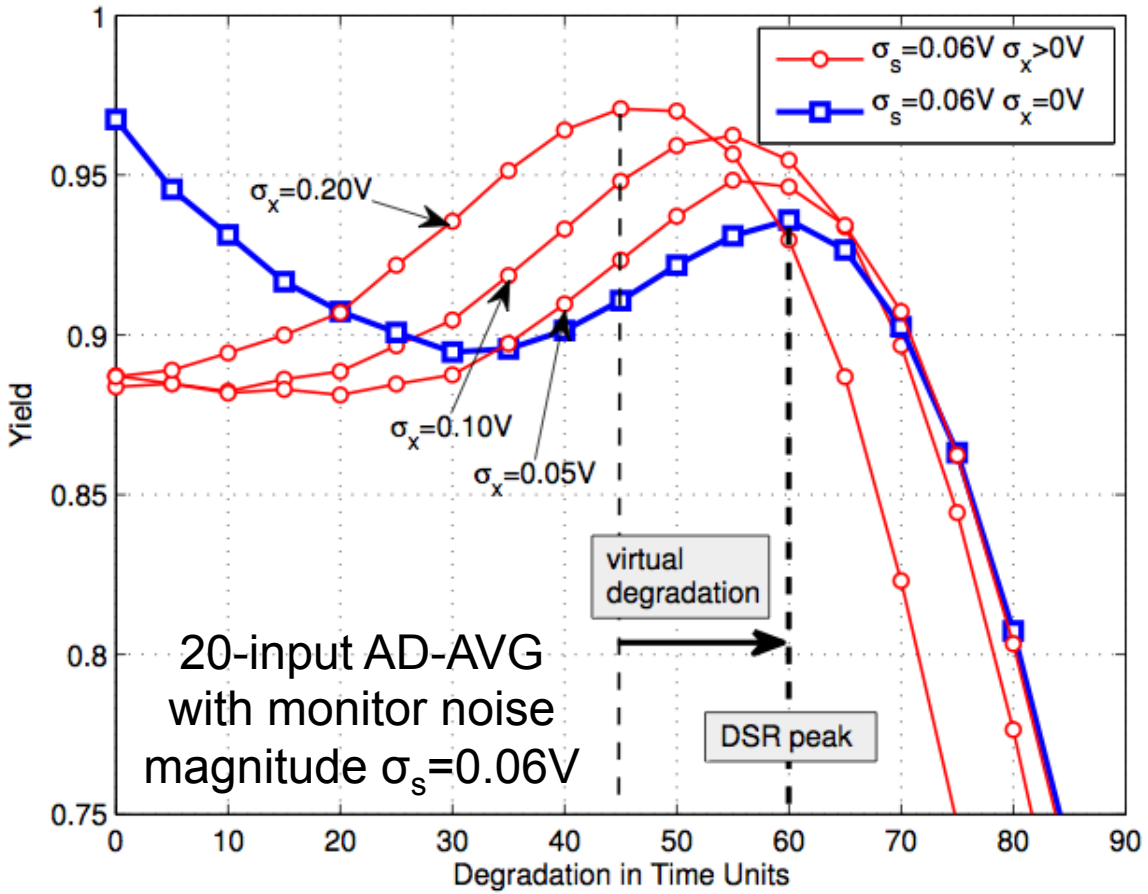
Induced DSR



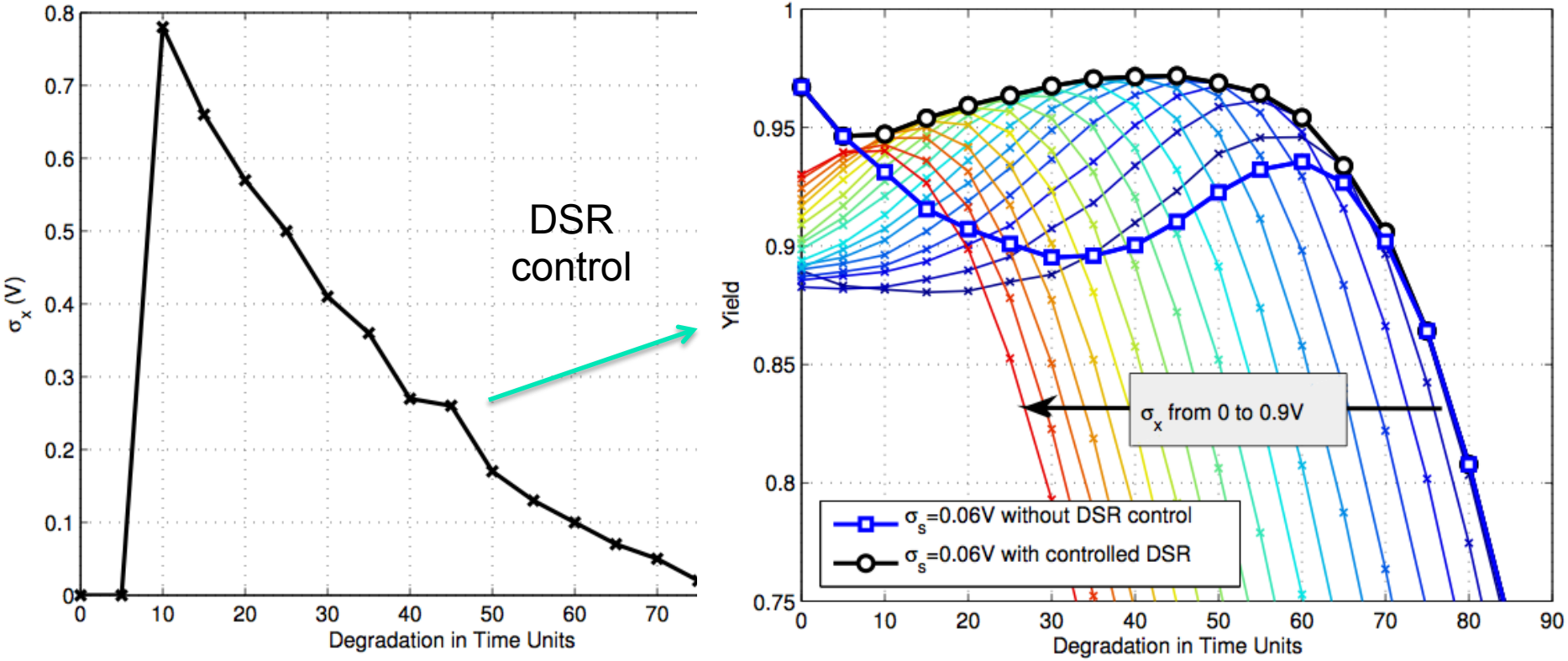
Input noise injectors $\varepsilon_i \sim N(0,\sigma_x)$ to create the DSR peak stochastic conditions regardless of the degradation level.

- N. Aymerich, S.D. Cotofana, and A. Rubio, "Controlled Degradation Stochastic Resonance in Adaptive Averaging Cell based Architectures", IEEE Transactions on Nanotechnology, pp. 888-896, Vol. 12, No. 6, November 2013.

Induced DSR


σs=0.06V σx>0V
σs=0.06V σx=0V
σx=0.20V
σx=0.10V
σx=0.05V
virtual degradation
DSR peak
20-input AD-AVG with monitor noise magnitude σs=0.06V
Yield
Degradation in Time Units
1
0.95
0.9
0.85
0.8
0.75
0
10
20
30
40
50
60
70
80
90

Induced DSR



Applying the correct amount of input noise we can move along the involute of the colored curves and obtain a yield even higher than that provided by the DSR peak.

Conclusions

- Nano-Era
- Opportunities & Challenges
- Alternative/Unorthodox Avenues
- Noise/Fluctuations can Facilitate and not Impede

And the answer is …