Timing Error Analysis of Flooded LDPC Decoders

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Innovative Reliable Chip Designs from Low-Powered Unreliable Components

Outline

- Related work
- Motivation
- LDPC decoder architecture
- Evaluation framework & methodology
- Faulty decoders under BIAWGN
- Faulty decoders under BSC
- Conclusions

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Related Work

- Theoretical analysis of faulty LDPC decoders
  - C/C++ or Matlab LDPC decoder models
  - Simple probabilistic errors
- Wide range of decoding algorithms
  - One step majority logic decoding – [Chilappagari06]
  - Gallagher-A decoding – [Varshney11]
  - Gallagher-B decoding – [Yazdi13]
  - Min-Sum decoding – i-Risc project
  - FAID decoding – i-Risc project

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Motivation

- Decoding algorithm ≠Decoder implementation
  - Wide range of architectural and implementation choices for the same decoding algorithm
    - Ex: parallelism degree at decoder level, parallelism degree at computational node level, message storage, pipelining, etc
  - Influence of probabilistic errors on decoding performance of a LDPC decoder architecture
- Probabilistic timing errors
  - Fault map highly depend on implementation choices
  - Error probability depends on the delay associated to each path

Motivation

- Contributions
  - The analysis is performed on an RTL description of an LDPC decoding architecture
  - Accurate timing error modeling for sub-powered LDPC decoder
  - Conclusion
    - Estimate of potential overclocking applicable to an LDPC decoder architecture
      - Throughput increase via overclocking

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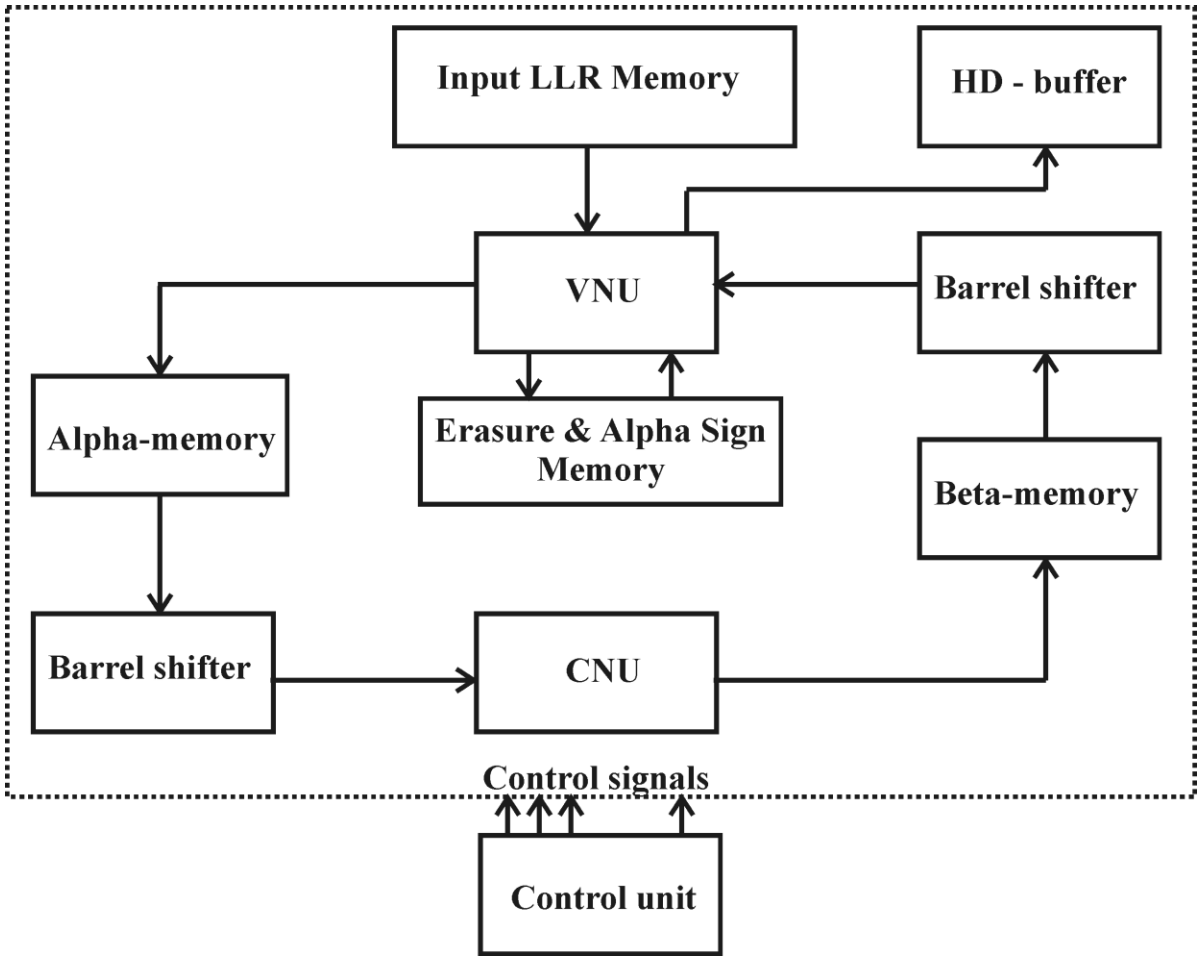
LDPC decoding architecture

- LDPC decoder parameters
  - (3,6)-regular QC-LDPC code
  - 1296 bits – codeword
  - Circulant size – 54
  - Flooded decoding
  - Early termination
  - Decoding algorithms:
    - MS, SCMS – (4,6) quantization
    - FAID – 3 bits quantization

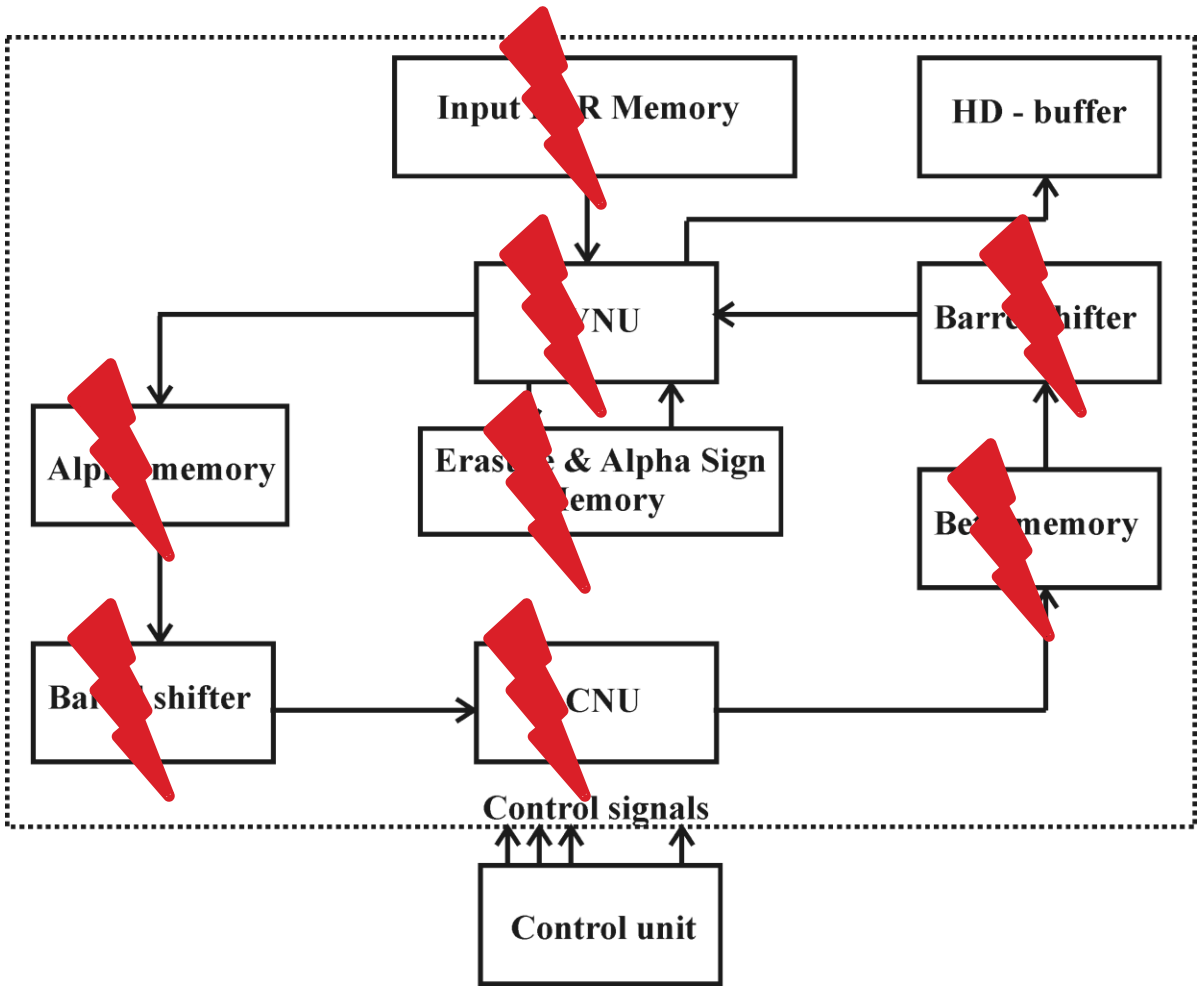
LDPC decoding architecture

- Serial processing messages at computational node (VNU/CNU) level
  - Reduction in memory access ports
- Parallel processing at B matrix row/column level
  - Increase in throughput
- B matrix rows and columns are processed in serial

LDPC decoding architecture



LDPC decoding architecture



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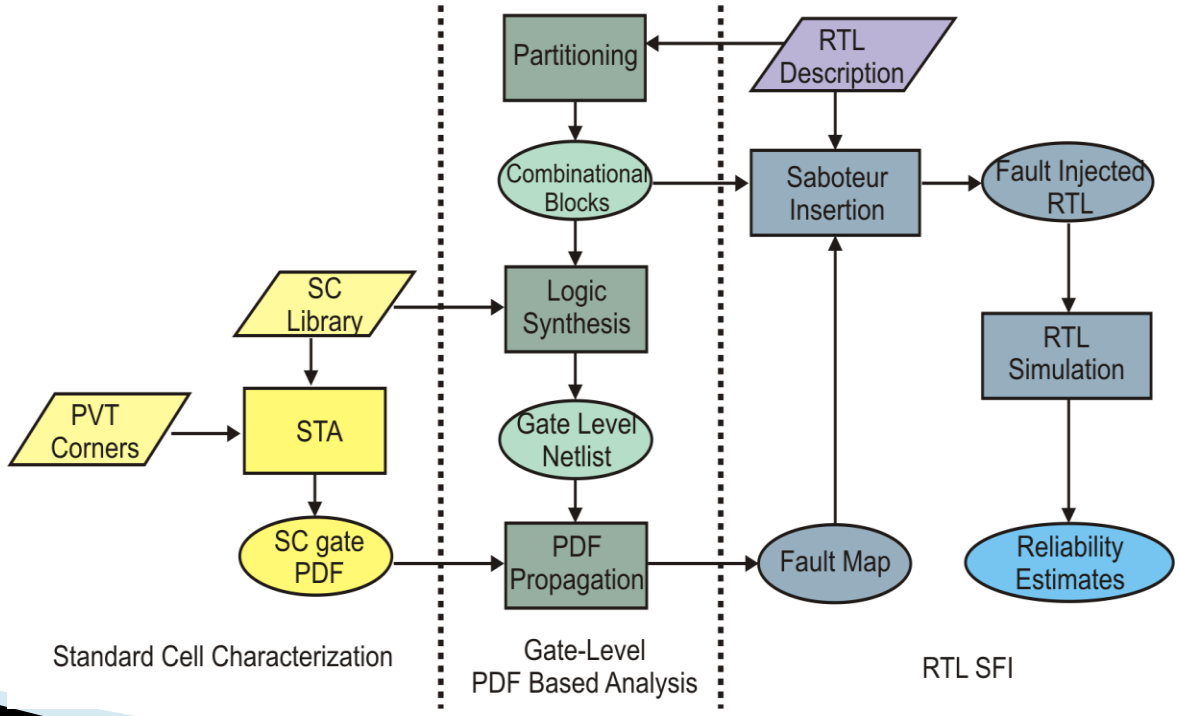
Evaluation Framework & Methodology

- Three layer evaluation methodology
  - Probabilities associated to each combinational primary output (PO) dependent on the PO delay

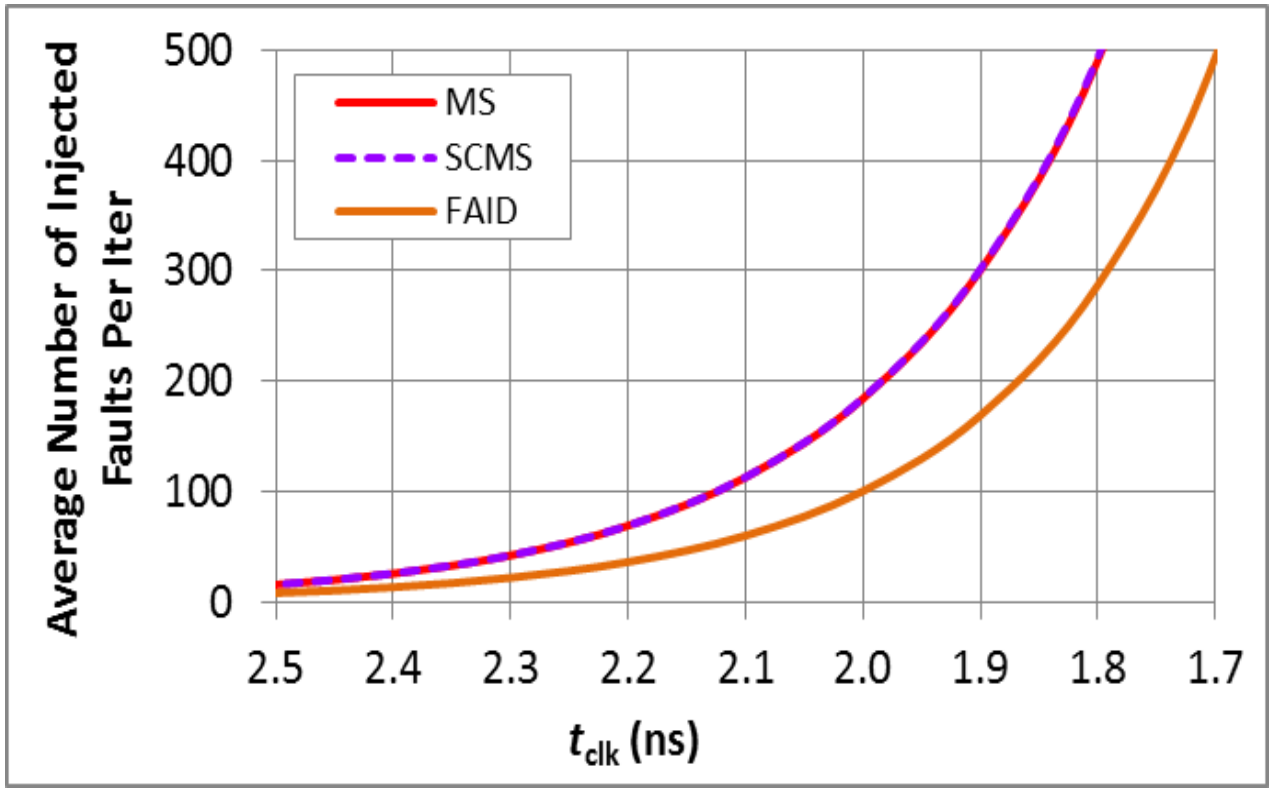


Evaluation Framework & Methodology

Average Probabilities for Considered Blocks

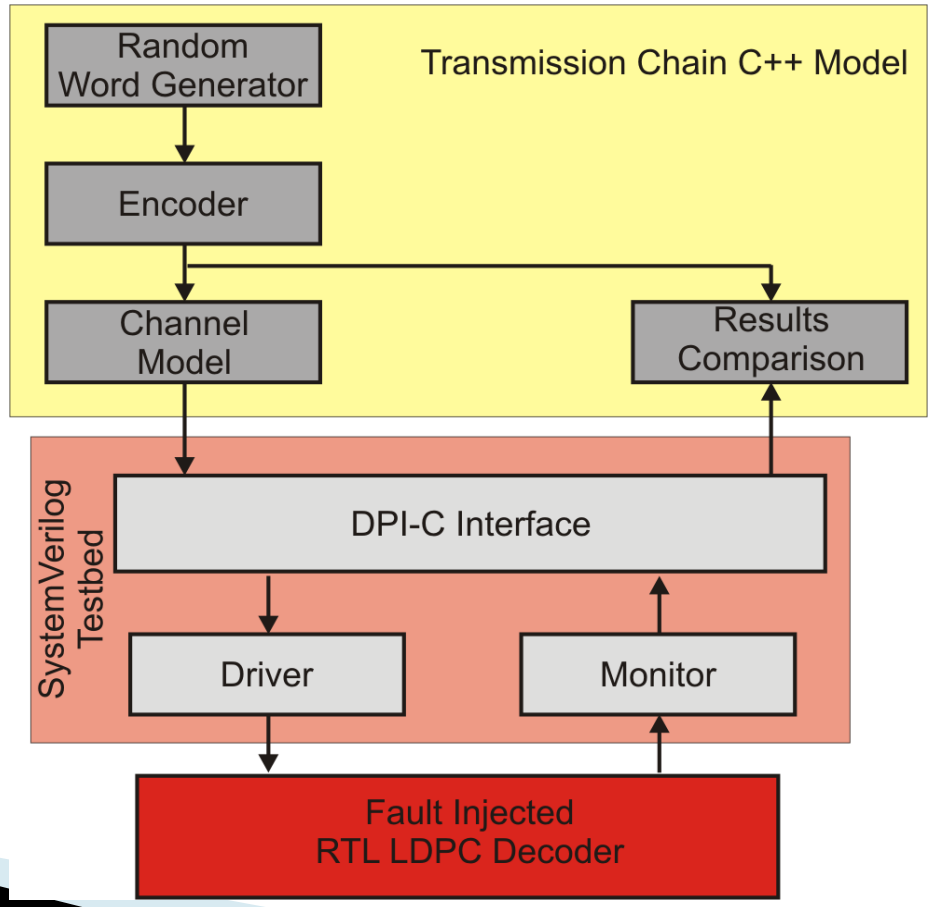
Clock Period (ns)	Mem	BS	MS/ SCMS CNU	MS VNU	SCMS VNU	FAID CNU	FAID VNU
5.50	0.00 E+00	0.00 E+00	1.28 E-10	0.00 E+00	0.00 E+00	9.70 E-11	0.00 E+00
4.00	0.00 E+00	0.00 E+00	3.51 E-07	3.14 E-08	2.47 E-08	2.66 E-07	2.26 E-09
2.50	9.64 E-07	2.79 E-06	6.05 E-04	1.92 E-04	1.51 E-04	4.58 E-04	4.61 E-05
2.20	1.28 E-05	2.71 E-05	2.33 E-03	9.94 E-04	7.81 E-04	1.76 E-03	3.12 E-04
1.90	1.60 E-04	2.62 E-04	8.13 E-03	4.80 E-03	3.77 E-03	6.18 E-03	1.98 E-03
1.70	8.28 E-04	1.17 E-03	1.75 E-02	1.30 E-02	1.02 E-02	1.33 E-02	6.48 E-03

Evaluation Framework & Methodology



Evaluation Framework

- Comparison with encoded data rather than comparison with correct LDPC decoder



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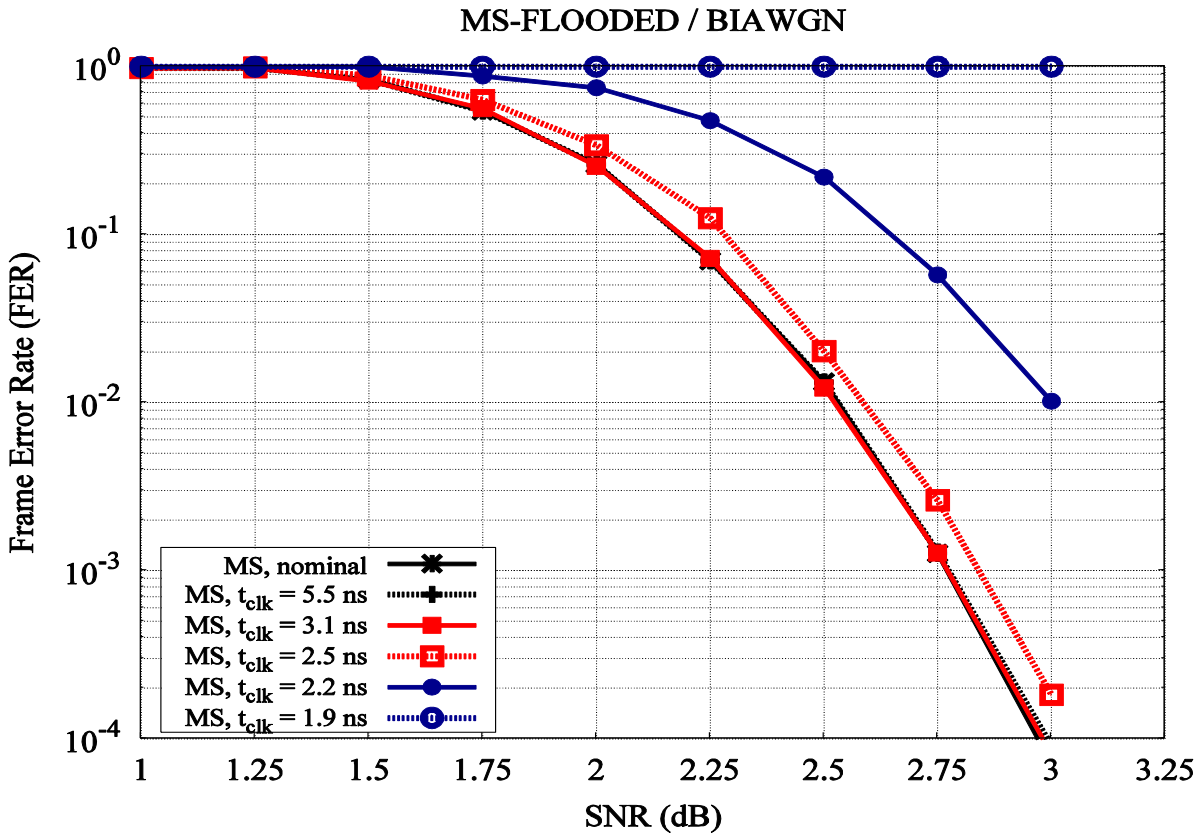
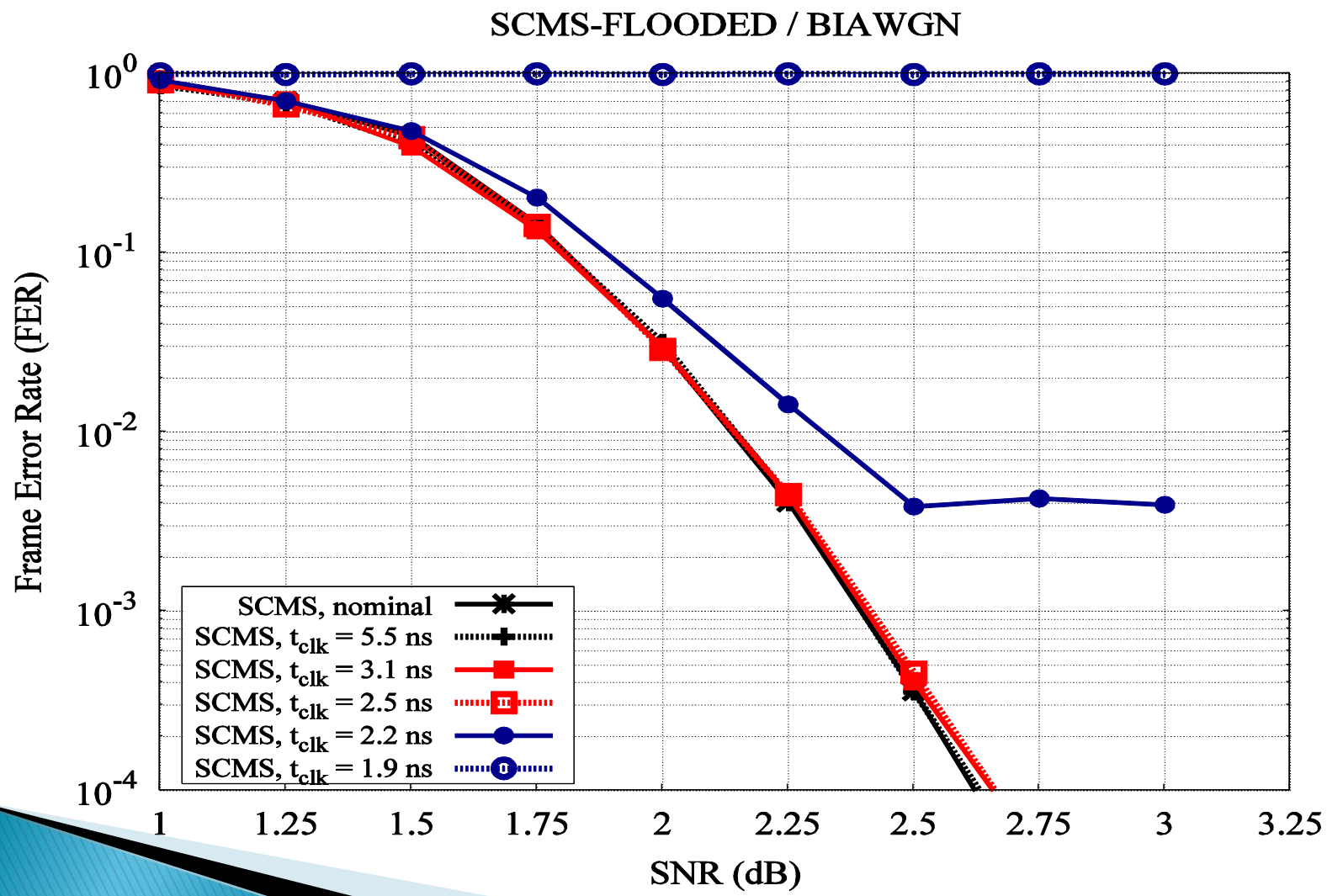
MS Under BIAWGN



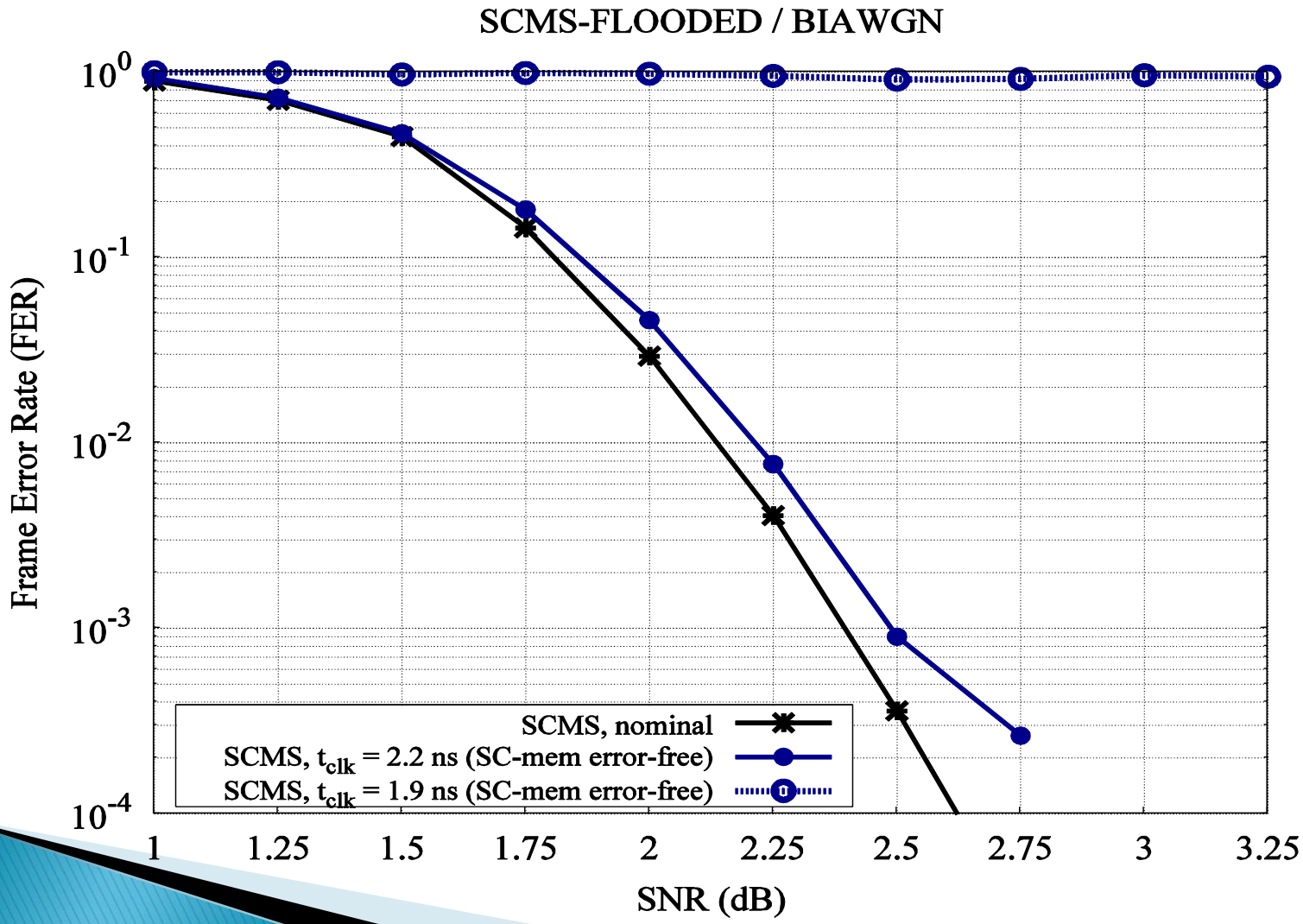
SCMS Under BIAWGN

- Faulty additional memories



SCMS Under BIAWGN

- Non-faulty additional memories



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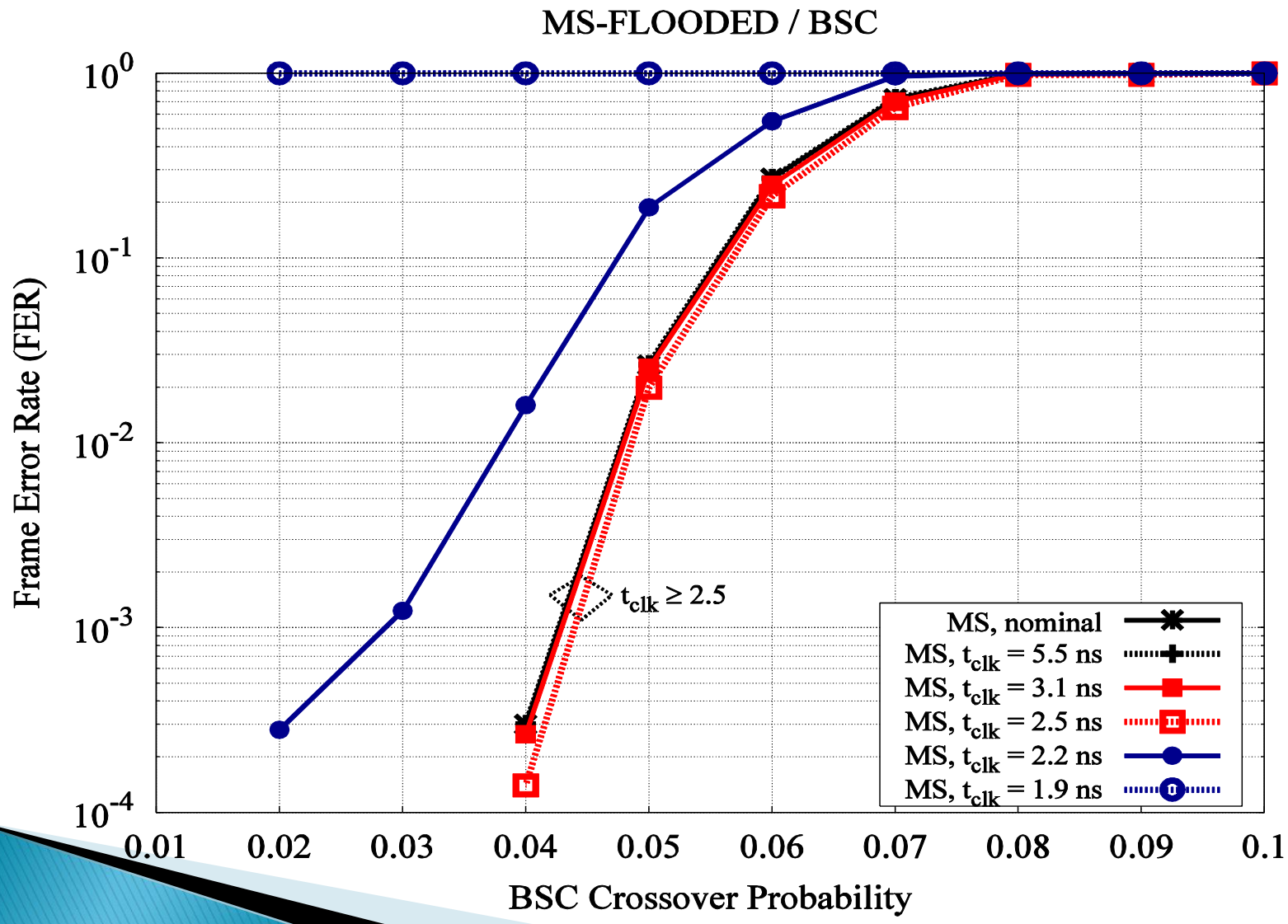
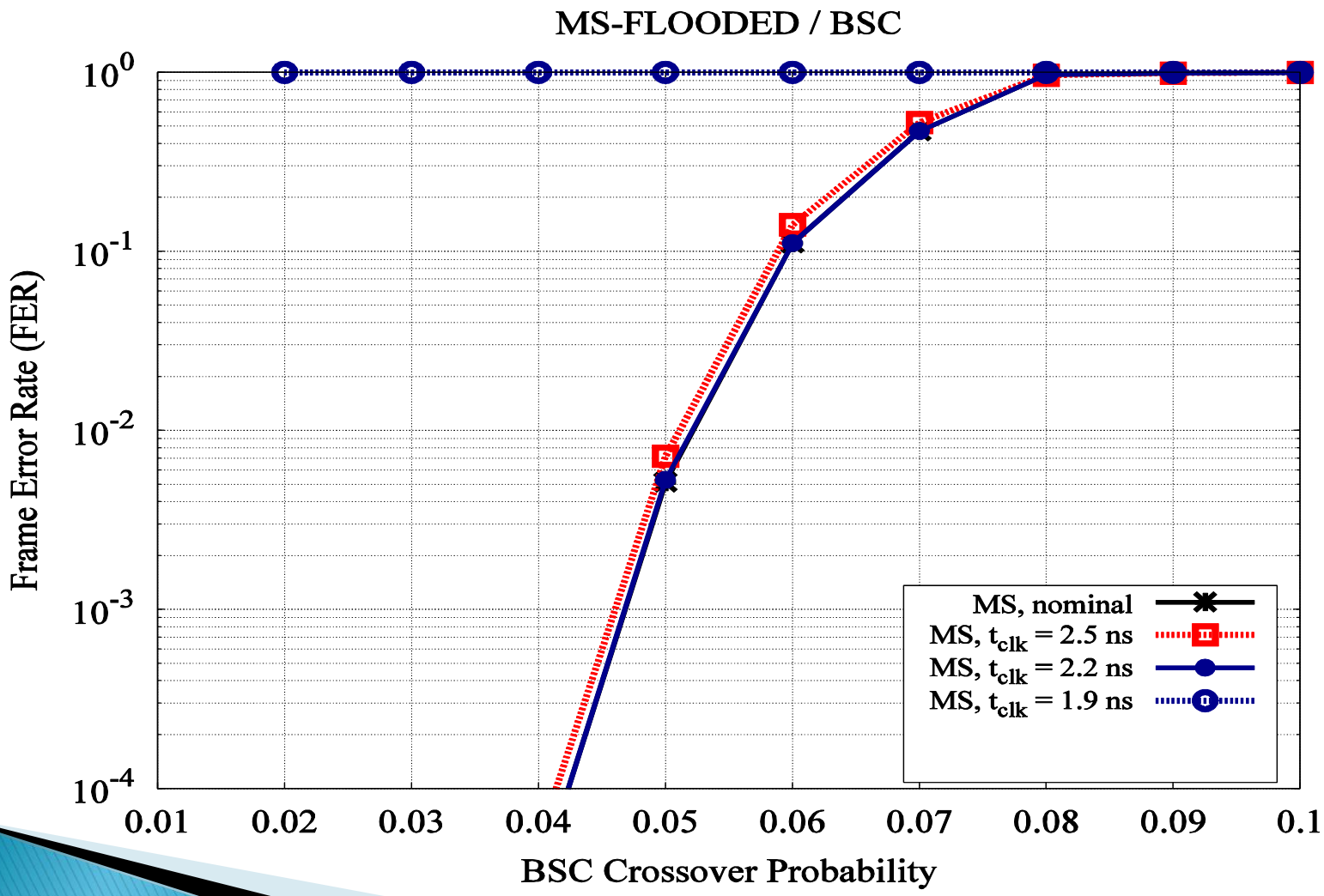
MS Under BSC

- Gain factor 3



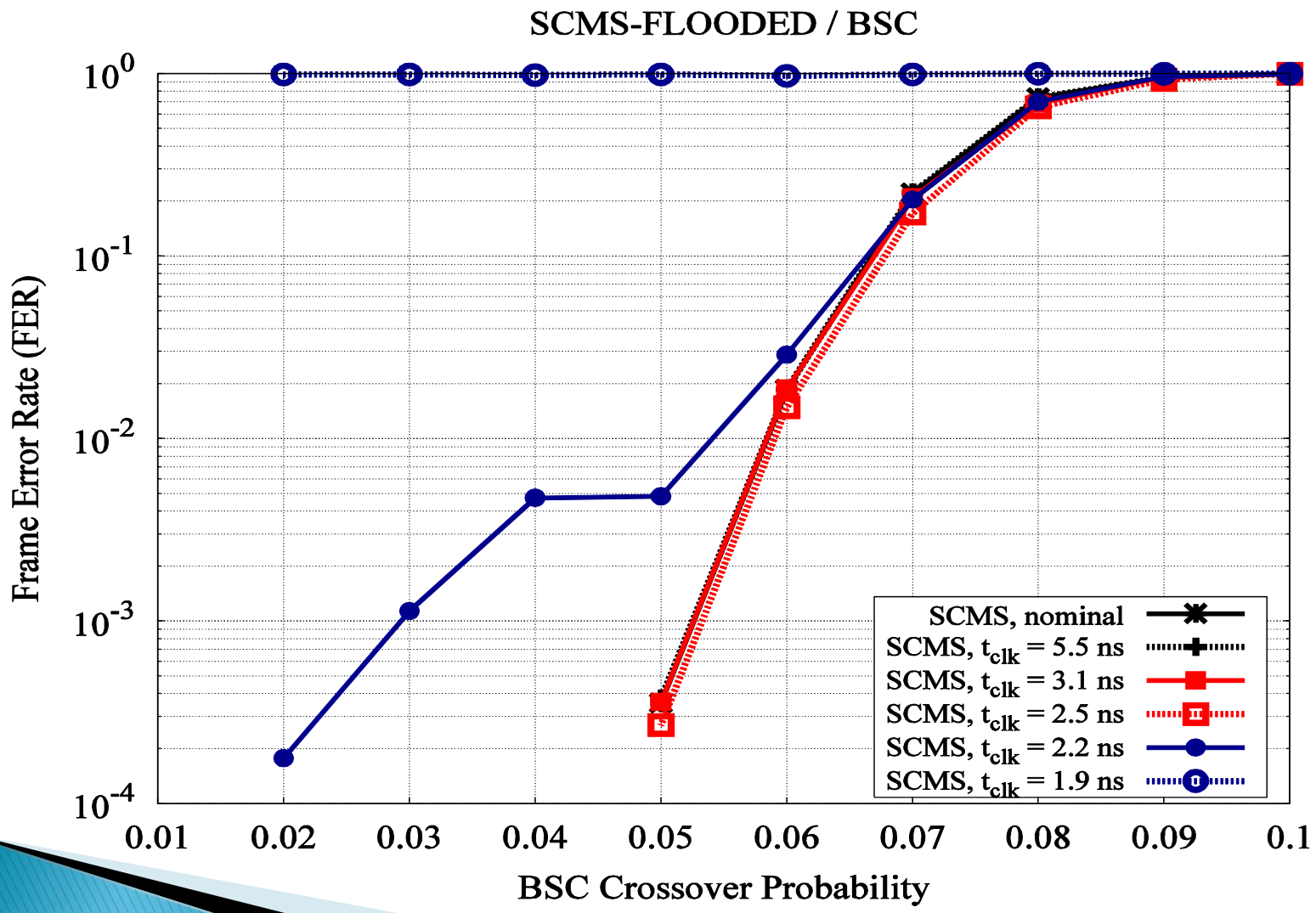
MS Under BSC

- Gain factor 4



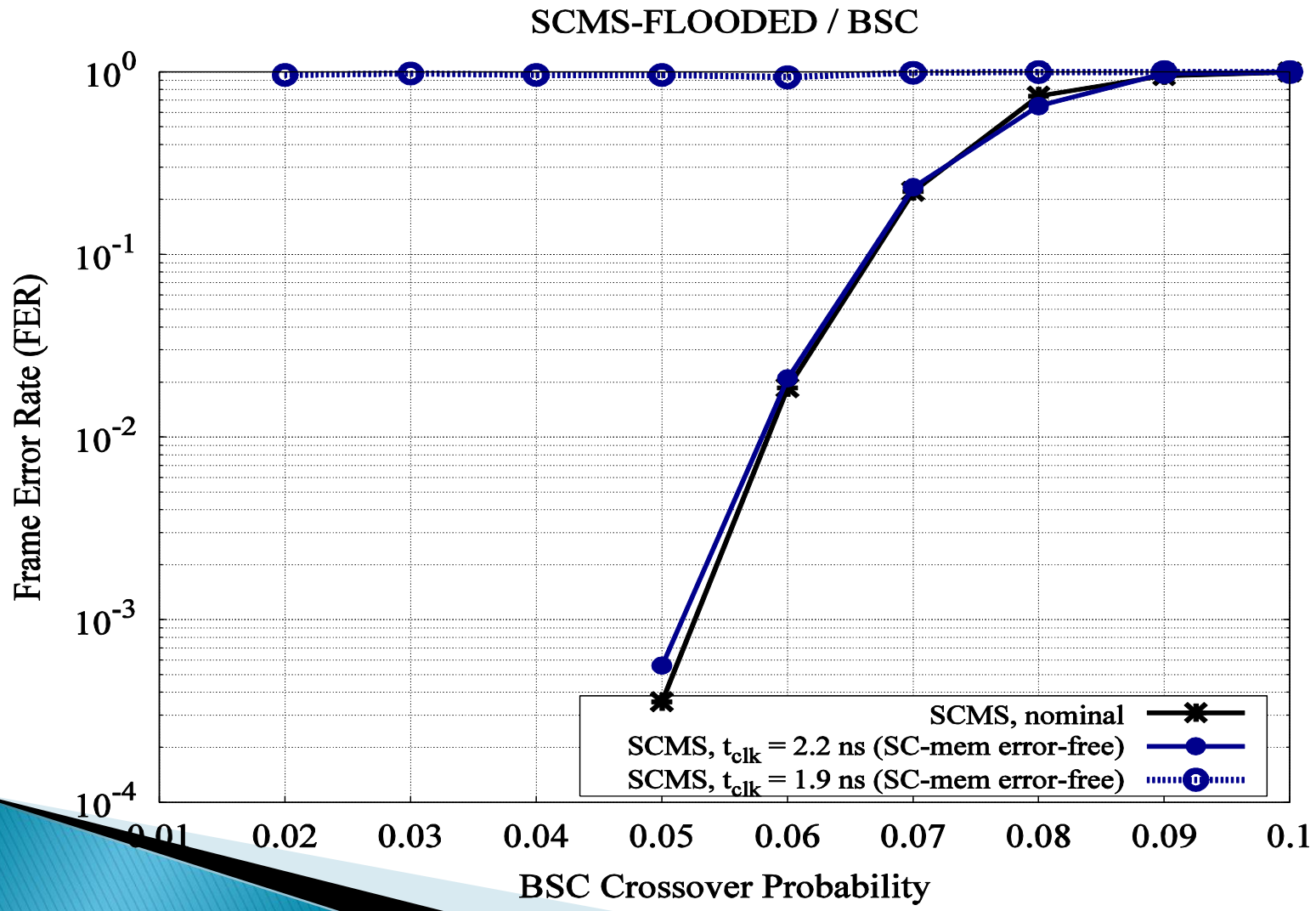
SCMS Under BSC

- Faulty additional memories

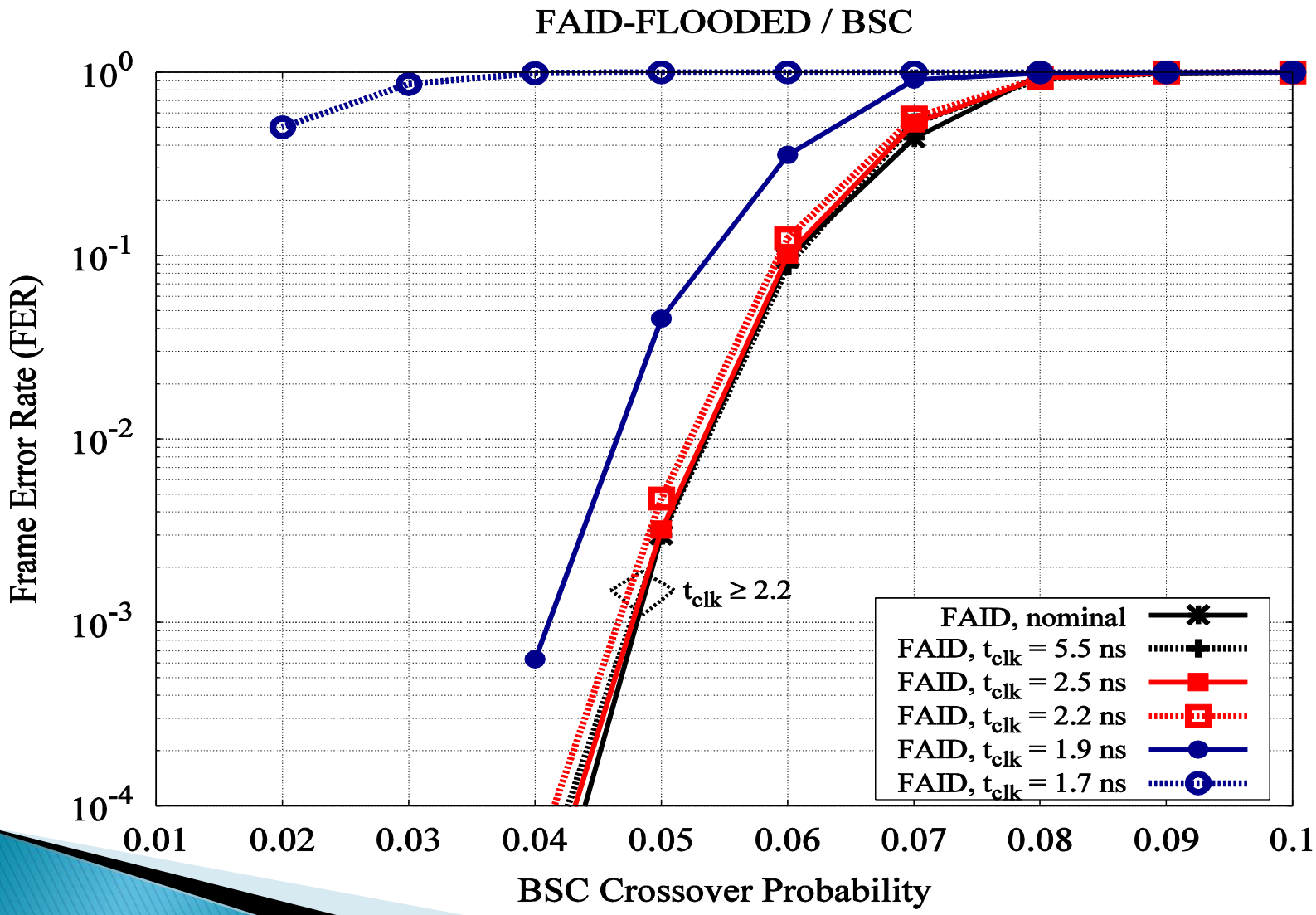


SCMS Under BSC

- Non-faulty additional memories



FAID Under BSC



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Conclusions

- LDPC decoder capability of correcting errors in their internal data-path
- Influence of the errors in the two additional memories of SCMS
- Influence of gain factor in MS for BSC
- FAID ability to withstand higher clock frequencies (it has lower fault probabilities)
- Throughput increase via overclocking
  - 70%-150% increase by overclocking


SEVENTH FRAMEWORK
PROGRAMME


i-RISC
innovative chip design

Thank You