
Finite-Alphabet Iterative Decoders Robust to Faulty Hardware

Elsa Dupraz¹, David Declercq¹, Bane Vasić² and Valentin Savin³

¹ETIS - ENSEA / Univ. Cergy-Pontoise / CNRS

²ECE department, University of Arizona

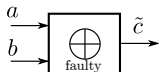
³CEA-LETI

Research reported in this presentation was supported by the Seventh Framework Programme of the European Union under Grant Agreement number 309129 (i-RISC project)

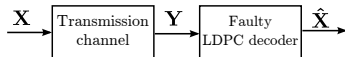
Introduction

Nowadays in electronic devices

- Important **chip size reduction**, increase in **integration factors**
- **Computation units** much more **sensitive to noise**
- Hardware assumed to be **faulty**



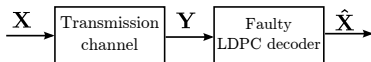
$$p_{\text{Xor}} = P(\tilde{c} \neq a \oplus b)$$



Context

LDPC decoding on **faulty hardware**

Introduction



- Are LDPC decoders inherently robust to hardware noise?
 - Noisy Gallager A [Var11], B [VC07, HLD13, YCD13], E [HD13]
 - Noisy quantized min-sum decoder [NSD13, BSB14]
- What makes a decoder robust?

Objective

Design decoders **robust** to faulty hardware

Outline

- 1 FAIDs on faulty hardware
- 2 Decoders design
- 3 Simulation results

Outline

1 FAIDs on faulty hardware

2 Decoders design

3 Simulation results

The FAID framework [PDDV13]

BSC(α), finite message alphabet $\mathcal{M} = \{-L_S, \dots, L_S\}$, $y \in \{-C, +C\}$

- CN computation: $\Phi_c(\mu_1, \dots, \mu_{d_c-1}) = \prod_{j=1}^{d_c-1} \text{sign}(\mu_j) \min_j |\mu_j|$
- VN computation: $\Phi_v(\eta_1, \dots, \eta_{d_v-1}, y_n)$

η_1/η_2	$-L_3$	$-L_2$	$-L_1$	0	$+L_1$	$+L_2$	$+L_3$
$-L_3$	$-L_3$	$-L_3$	$-L_3$	$-L_3$	$-L_3$	$-L_3$	$-L_1$
$-L_2$	$-L_3$	$-L_3$	$-L_3$	$-L_3$	$-L_2$	$-L_1$	L_1
$-L_1$	$-L_3$	$-L_3$	$-L_2$	$-L_2$	$-L_1$	$-L_1$	L_1
0	$-L_3$	$-L_3$	$-L_2$	$-L_1$	0	0	L_1
L_1	$-L_3$	$-L_2$	$-L_1$	0	0	L_1	L_2
L_2	$-L_3$	$-L_1$	$-L_1$	0	L_1	L_1	L_3
L_3	$-L_1$	L_1	L_1	L_1	L_2	L_3	L_3

Defines a large collection of mappings

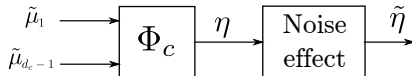
- APP computation: $\Phi_a(\eta_1, \dots, \eta_{d_v}, y) = \sum_{j=1}^{d_v} \eta_j + y$

Objective

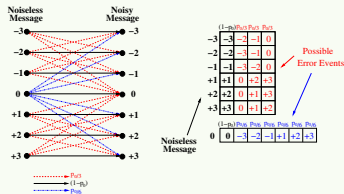
Design mapping Φ_v for **robustness** to hardware errors

Error Model in the decoder

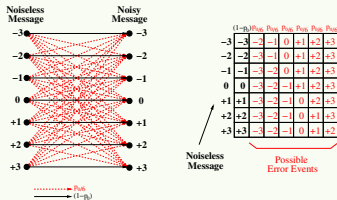
- Noise effect assumed to be at the end of function computation



Sign-Preserving (SP) model



Full-Depth (FD) model



VN: p_v

CN: p_c

APP: p_a

Outline

- 1 FAIDs on faulty hardware
- 2 Decoders design**
- 3 Simulation results

Noisy Density evolution¹

- **Assumptions:** Infinite codeword length, cycle-free graph, all-zero codeword

Density evolution

- Recursion on the probabilities of the messages ($\ell > 1$)

$$\text{CN output } \mathbf{p}_\eta^{(\ell)} = \mathcal{F}_{\Phi_c}(\mathbf{p}_\mu^{(\ell-1)}, p_c) \quad \text{VN output } \mathbf{p}_\mu^{(\ell)} = \mathcal{F}_{\Phi_v}(\mathbf{p}_\eta^{(\ell)}, \alpha, p_v, \Phi_v)$$

- Probabilities of the APP

$$\text{APP output } \mathbf{p}_{\text{app}}^{(\ell)} = \mathcal{F}_{\Phi_a}(\mathbf{p}_\eta^{(\ell)}, \alpha, p_a)$$

Error probability

- $$P_e^{(\ell)}(\alpha, p_v, p_c, p_a, \Phi_v) = \frac{1}{2} p_{\text{app},0}^{(\ell)} + \sum_{k < 0} p_{\text{app},k}^{(\ell)}$$

¹Elsa Dupraz, David Declercq, Bane Vasic, Valentin Savin, *Analysis and Design of Finite Alphabet Iterative Decoders Robust to Faulty Hardware* Submitted at IEEE Trans. on Comm., October 2014

Functional threshold¹

If exists, $P_e^{(+\infty)}(\alpha, p_v, p_c, p_a, \Phi_v) = \lim_{\ell \rightarrow \infty} P_e^{(\ell)}(\alpha, p_v, p_c, p_a, \Phi_v)$

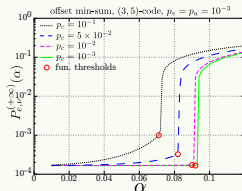
Noiseless threshold [RU01]

max α s.t. $P_e^{(+\infty)}(\alpha, p_v, p_c, p_a, \Phi_v) = 0$

Condition impossible to reach in general in the noisy case

Functional threshold

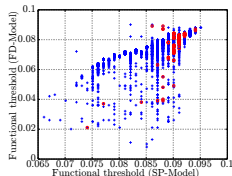
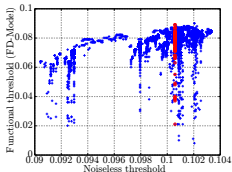
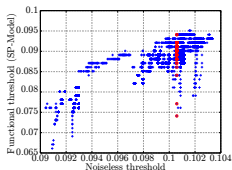
Transition between low level and high level of error probability



¹Christiane L. Kameni Ngassa, Valentin Savin, Elsa Dupraz, David Declercq, *Density Evolution and Functional Threshold for the Noisy Min-Sum Decoder* IEEE Trans. on Comm., May 2014

FAIDs design¹

- collection of $N_D = 5291$ FAIDs optimized for low error-floor
- **Functional threshold** for each of the N_D FAIDs



For each model, select two decoders

- $\Phi_V^{(\text{robust})}$: **minimizes** discrepancy between noiseless and noisy th.
- $\Phi_V^{(\text{non-robust})}$: **maximizes** discrepancy between noiseless and noisy th.

¹Elsa Dupraz, David Declercq, Bane Vasic, Valentin Savin, *Analysis and Design of Finite Alphabet Iterative Decoders Robust to Faulty Hardware* Submitted at IEEE Trans. on Comm., October 2014

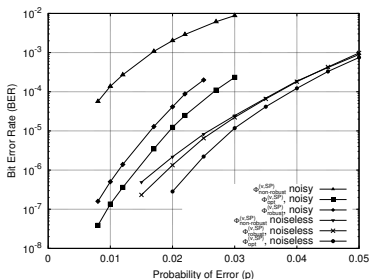
Outline

- 1 FAIDs on faulty hardware
- 2 Decoders design
- 3 Simulation results**

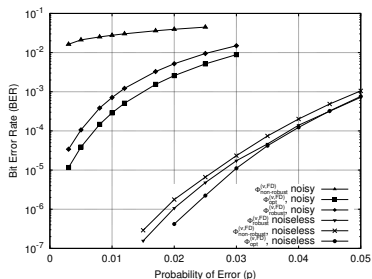
Finite-length simulation results

(155,93) Tanner code, $d_v = 3$, $d_c = 5$

SP-Model, $p_v = p_c = p_a = 0.05$



FD-Model, $p_v = p_c = p_a = 0.02$



Conclusions

■ Summary

- Functional threshold to characterize the asymptotic behavior of the noisy decoders
- Design of FAIDs robust to noise introduced by the faulty hardware

■ Perspectives

- Analysis of more accurate error models (Not sign-preserving, not symmetric, etc.)
- Other applications: reliable storage and function computation

-
- [BSB14] A. Balatsoukas-Stimming and A. Burg.
Density evolution for min-sum decoding of LDPC codes under unreliable message storage.
IEEE Communications Letters, PP(99):1–4, 2014.
- [HD13] C.H. Huang and L. Dolecek.
Analysis of finite-alphabet iterative decoders under processing errors.
In *IEEE International Conference on Acoustics, Speech and Signal Processing*, pages 5085–5089, 2013.
- [HLD13] C-H. Huang, Y. Li, and L. Dolecek.
Gallager B LDPC decoder with transient and permanent errors.
In *IEEE International Symposium on Information Theory Proceedings*, pages 3010–3014, 2013.
- [NSD13] C. Kameni Ngassa, V. Savin, and D. Declercq.
Min-Sum-based decoders running on noisy hardware.
In *Proc. IEEE GLOBECOM 2013*, Dec. 2013.
- [PDDV13] S.K. Planjery, D. Declercq, L. Danjean, and B. Vasic.
Finite alphabet iterative decoders-part I: decoding beyond belief propagation on the binary symmetric channel.
IEEE Transactions on Communications, 61(10):4033–4045, 2013.
- [RU01] T. J. Richardson and R. Urbanke.
The capacity of low-density parity-check codes under message-passing decoding.
IEEE Transactions on Information Theory, 47(2):599–618, Feb. 2001.
- [Var11] L.R. Varshney.
Performance of LDPC codes under faulty iterative decoding.
IEEE Transactions on Information Theory, 57(7):4427–4444, July 2011.

-
- [VC07] B. Vasic and S.K. Chilappagari.
An information theoretical framework for analysis and design of nanoscale fault-tolerant memories based on low-density parity-check codes.
IEEE Transactions Circuits Systems I, Regular Papers, 54(11):2438–2446, Nov. 2007.
- [YCD13] S. Yazdi, H. Cho, and L. Dolecek.
Gallager B decoder on noisy hardware.
IEEE Transactions on Communications, 61(5):1660–1673, 2013.