i-RISC Workshop Program

Opening

9:00-9:30

The i-RISC Project: Innovative Reliable Chip Designs from Low-Powered Unreliable Components
Valentin Savin (CEA) & Sorin Cotofana (TUD)

Abstract: The i-RISC project addresses the problem of reliable computing with unreliable components, which is a crucial issue for the long-term development of computing technology. The novelty of the proposed research comes from the synergistic utilization of information theory and coding techniques, traditionally utilized to improve the reliability of communication systems, and circuit and system theory and design techniques in order to create reliable/predictable hardware.

Fault Tolerant Algorithms for Error-Correction

9:30-10:00

Analysis and Design of Min-Sum-based Decoders Running on Noisy Hardware
Christiane Kameni-Ngassa, Valentin Savin (CEA), & David Declercq (ENSEA)

Abstract: In this talk we investigate the robustness of the LDPC decoders in the presence of an additional source of noise at the circuit level. To this end, we introduce a new error model approach and carry out the "noisy" density evolution analysis of the fixed-point Min-Sum decoding. Then, for different parameters of the noisy components of the decoder, we determine the range of the signal-to-noise ratio values for which the decoder is able to achieve a target bit error rate performance. Finally, we evaluate the finite-length performance of the Min-Sum and two other Min-Sum-based decoders running on noisy hardware.

10:00-10:30

Performance of Finite Alphabet Iterative Decoders (FAID) Under Faulty Hardware
David Declercq, Shiva Planjery (ENSEA), & Bane Vasic (ELFAK)

Abstract: In this talk, the FAID decoders for binary LDPC decoding will be presented and analyzed under simple error model of faulty hardware implementation. A statistical analysis on a large collection of FAID decoding rules will be used to stress the fact that some particular update functions are more robust than others under faulty hardware, while still being efficient in terms of error correction. This analysis serves as a first basis for the optimized design of specific LDPC decoders, which are both powerful and robust to faulty hardware.

10:30 – 11:00 - Coffee Break

Reliable Data Storage and Transport

11:00-11:30

Bit-flipping Decoders for Fault-Tolerant Memories
Bane Vasic, Srdjan Brkic, Predrag Ivanis, & Goran Djordjevic (ELFAK)

Abstract: In this talk we present a method for the design and analysis of fault-tolerant memories. Unlike traditional methods based on Taylor-Kuznetsov (TK) architecture, which rely on Gallager B algorithm, we use the bit flipping algorithm. We show the complexity reduction offered by this method and present a class of soft bit flipping algorithms.

11:30-12:00

The Analysis of Taylor-Kuznetsov Fault-Tolerant Memories Under Correlated Gate Failures
Srdjan Brkic, Predrag Ivanis, Goran Djordjevic, & Bane Vasic (ELFAK)

Abstract: In this talk we present a method for unreliable logic gates analysis in presence of correlated, data-dependent gate failures, described by Markov chain model. The presented probabilistic method is used for analysis of Taylor-Kuznetsov (TK) memory architectures constructed only by NAND logic gates.

12:00 – 13:30 - Lunch

Error Models & Energy Measures

13:30-14:00

Gate Level Simulated Fault Injection for Probabilistic CMOS Circuits
Sergiu Nimara, Alexandru Amaricai, Oana Boncalo (UPT), Jiaoyan Chen, & Emanuel Popovici (UCC)

Abstract: HDL based simulated fault injection represents one of the most common approaches for evaluating the reliability of fault tolerant circuits. It has the advantage that it presents good error modelling capability, while the reliability evaluation is applied to the same HDL source code used for the circuit design and implementation. In this presentation, we will investigate the possibility of applying simulated fault injection to probabilistic circuits. We will present a mutant based approach for gate level netlist, which models a wide range of probabilistic errors which appear in sub-powered CMOS circuits.

14:00-14:30

Interconnect Crosstalk Analysis in Sub-powered Integrated Circuits
Alexandru Amaricai, Oana Boncalo, & Sergiu Nimara (UPT)

Abstract: In this presentation, we investigate the influence of several physical parameters on the interconnect reliability in sub-powered circuits. The interconnects are analyzed using RLC networks, based on PTM interconnects models. We present the influence of the supply voltage, interconnect length, interconnect spacing and dielectric material on the crosstalk for switching wires. The main goal is to determine the logic level voltage alteration on victim lines, due to crosstalk in interconnects.

14:30-15:00

Delay Relevant Reliability of CMOS Circuits
Chen Jiaoyan, Christian Spagnol, Satish Kumar, & Emanuel Popovici (UCC)

Abstract: Ultra-low power supply, i.e. near/sub threshold region, is a promising alternative in power reduction. In this presentation, we describe and evaluate some delay approximation models. . Propagation delay in CMOS circuits becomes even harder to estimate due to the statistical variations on many aspects of the production process. Accurate and simplified delay model could significantly enhance the feasibility of delay relevant reliability prediction. Great flexibility to different power supply and different types of distributions for VTH are demonstrated. The capability of the proposed method has been investigated and it is shown how linear summation can be implemented to propagate key parameters in our model. Average deviations of only 0.8% and 1.2% are achieved for a number of circuits including Majority Voter and XOR gate respectively, when compared to complete Monte Carlo simulation in HSPICE.

15:00 – 15:30 - Coffee Break

Reliable Function Synthesis and Design

15:30 – 16:00

A systematic Approach for Reliability Evaluation of Combinational Circuits
Christian Spagnol, Satish Kumar, Chen Jiaoyan, & Emanuel Popovici (UCC)

Abstract: Reliability and its modeling have become critical issues for deep sub-micron technology based designs. In this talk, we present some probabilistic methodologies to compute the reliability of combinational circuits. An open source logic synthesis tool called 'abc' has been used for automating the flow. We address various issues including node reliability under unreliable conditions, impact of reconvergent fan-out and some insights into error bounds.

16:00 – 17:00
Reliability Assessment Framework for Large Scale Causal Logic Networks
Nicoleta Cucu-Laurenciu & Sorin Cotofana (TUD)

Abstract: Accurate and fast circuit reliability assessment is needed at design-time, to enable a reliability driven synthesis process and to allow the construction of reliable circuits out of unreliable and/or underpowered MOSFETs and/or emerging nano-devices. To this end, we present a hierarchical framework with the following abstraction layers: (i) device-level - standard cells characterization with ancillary device-level Monte Carlo based reliability estimates, and (ii) gate-level – variational probabilistic inference in large causal logic networks, in order to derive the circuit failure probability for given gate error and environmental aggression profiles.

17:00 -17:30

Open Discussion and Closing Remarks

Moderators: Valentin Savin (CEA) & Sorin Cotofana (TUD)

Affiliations

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