PROJECT PERIODIC REPORT

Grant Agreement number: 309129

Project acronym: I-RISC

Project title: Innovative Reliable Chip Designs from Low-Powered Unreliable Components

Funding Scheme: CP / CP-FP-INFSO

Date of latest version of Annex I against which the assessment will be made: 2012-10-05

Periodic report: **1st ☑ 2nd ☐ 3rd ☐ 4th ☐**

Period covered: **from 2013-02-01 to 2014-01-31**

Name, title and organisation of the scientific representative of the project's coordinator:

Dr. Valentin Savin

Commissariat à l'Energie Atomique et aux Energies Alternatives

17, Rue des Martyrs

38054 Grenoble, Cedex 9

France

Tel: +33-438 780 963

Fax: +33-438 785 159

E-mail: valentin.savin@cea.fr

Project website address: http://www.i-risc.eu/

FP7-ICT-2011-C / FET-OPEN / 309129

PROJECT PERIODIC REPORT

Publishable Summary

3.1 Publishable summary

3.1.1 Context and objectives

The on-going miniaturization of data processing and storage devices and the low-energy consumption imperative can only be sustained through low-powered components. However, lower supply voltages combined with the intrinsic device variations introduced by emerging nanoelectronic device fabrication process make them inherently unreliable. As a consequence, the nanoscale integration of reliable chips built out of unreliable components emerged as one of the most critical challenges for the next-generation electronic circuit design. To make such nanoscale integration economically viable, new solutions for efficient fault-tolerant data processing and storage must be investigated.

The i-RISC project targets a foundational breakthrough towards reliable, fault-tolerant chip design from unreliable components, which is a crucial issue for the computing technology long-term development. The research novelty emerges from the synergistic utilization of (1) information theory and coding techniques, traditionally utilized to improve the communication systems reliability and (2) circuit and system theory and design techniques, in order to create reliable/ predictable hardware. The aim is to enable the development of innovative fault-tolerant solutions at both circuit- and system-level that are fundamentally rooted in mathematical models, algorithms, and techniques from information and coding theory.

3.1.2 Proposed approach

Error correcting codes utilization proved to be a fundamental information theory cornerstone, providing an efficient solution to the problem of reliable communication over unreliable channels. The i-RISC project is aimed at shifting the error correction paradigm from communication to computing systems. The central i-RISC target is to acquire error-free computing with error-prone components. i-RISC proposes to tackle this problem by detouring error correcting codes from their traditional use, such that they provide efficient protection against circuit-induced errors. To make such an approach viable, both fundamental and exploratory research must be conducted at different circuit or system levels.

A first level of research is required to characterize and optimize the circuit probabilistic behaviour. The goal is to develop error models that cover the effects of chip sub-powering, production imperfections, environmental deterioration, and aging. Moreover it is necessary to analyse the effect of energy consumption, clock frequency, environmental condition, and area requirements on the circuit error probability.

A second level of research is required to advance the knowledge and understanding of error-correcting codes in the context of unreliable devices. In contrast to the traditional use of error correcting codes, faulty hardware represents a new error source that can perturb the encoding and/or decoding process. It is then crucial to analyse and design error correcting encoders and decoders able to provide reliable error correction even if they are made out of unreliable components.

A third level of research is required to investigate the design of fault tolerant error correction techniques that can contribute to the reliable storage and transfer of the digital information throughout the chip. This relies on the well-known principle of encoded information processing, but the codec must be made compliant with the requirements of reliable interconnects and memories.

A fourth level of research is required to identify solutions that allow combining the codec architecture with the hardware it protects. i-RISC will study potential links between graph representations of digital circuits and of error correcting codes, in order to generate fault tolerant implementation of the circuit logical functionality.

The above research levels are strongly interacting and eventually converge to an effective fault-tolerance solution, which allows circuit multi-objective optimization, with respect to size, energy consumption, latency, and reliability. The optimization is taking into account the design of the fault-tolerant decoder architecture, its integration into the structural description of the circuit, and the unreliable component error models. Finally, the effectiveness of the proposed solutions will be demonstrated through the implementation of fault tolerant decoders and of a number of benchmark circuits.

3.1.3 Description of the work performed since the beginning of the project

The project proposed accurate probabilistic fault models for CMOS circuits operating at very low power supply voltage values, based on a Dynamic Timing Analysis (DTA). Two analytical methods for reliability analysis of probabilistic circuits have been developed. The first one relies on an Inverse Gaussian (IG) distribution delay model, which allows accurate and fast reliability evaluation of probabilistic circuits. The second method employs a Markov chain based symbolic analysis methodology, which takes into account data dependencies. Markov chains have been used to describe both input and output dependent error models. Moreover, a variable reduction method has also been developed, in order to analyse gate net-lists composed of basic logic gates.

In order to address the reliability assessment of logic circuits represented by gate-level net-lists, the project also started developing the gate level simulated fault injection methodology. Existing Hardware Description Languages (HDL) based Simulated Fault Injection (SFI) frameworks and methodologies have been extended, so as to accommodate data dependent probabilistic errors. The proposed SFI methodology can accommodate different gate-level fault models and is targeted on the reliability estimation of gate-level net-lists generated during the logic synthesis process.

The project has further investigated noisy versions of several LDPC decoders: the finite precision Min-Sum (MS) decoder, a modified version of the MS decoder incorporating a dynamical correction of mis-convergence, called self-corrected MS (SC-MS), and more general decoders based on non-linear Boolean function for the message passing updates, called Finite Alphabet Iterative Decoders (FAID). Theoretical limits for the MS and FAID decoders under faulty hardware have been derived by using a noisy Density Evolution (DE) approach. The project has also focused on means to improve the decoder reliability, by protecting critical bits of the finite-precision computation flow within the decoding process. To this end, sign-preserving error models have been investigated, and their benefits have been demonstrated asymptotically through DE analysis, and verified at finite-lengths by Monte Carlo simulations.

Additionally, the project has also conducted a finite length statistical analysis of the different decoders. In particular, the noisy SC-MS decoder has been shown to provide nearly the same performance as the noiseless decoder, for a wide range of values of the hardware noise parameters. For FAID decoders, it has been shown that one can identify message passing update rules which are naturally more robust to transient errors, and more importantly, that the best update rules for the noisy case are not the same as the best update rules for the noiseless case.

The project has further investigated the design of fault-tolerant Taylor-Kuznetsov (TK) memory architectures based on structured LDPC codes. The influence of different code parameters, decoder structures and fault model parameters on the overall system performance has also been studied. A novel class of two-bit bit flipping (TBF) algorithms has been proposed, showing a significant improvement of the bit error rate performance, as compared to traditional bit flipping algorithms. The TBF decoder failures have been characterized by constructing the trapping set profile of the decoder, and it has been shown that different TBF decoders are capable of correcting different error patterns. The explicit construction of trapping set profiles allows rigorous selections of multiple TBF algorithms that can collectively correct a fixed number of errors with high probability.

As fast decoding convergence is an important issue for fault tolerant memories, the project has also proposed a novel class of fast convergence iterative decoders called decimation-enhanced FAIDs. The proposed technique is based on deactivating a carefully chosen number of nodes from the computation tree, which speed up the decoding process, while maintaining the same error correction performance. Furthermore, it has been proved that guaranteed error-correction could be achieved in a finite and small number of iterations. This represents a first result on guaranteed error-correction for advanced message-passing decoders, and hopefully will allow designing TK-memory architectures with guaranteed robustness properties.

The project has further focused on data structures and design flow for the systematic synthesis of reliable circuits. A number of data structures have been analysed and the And-Inverter-Graph (AIG) structure has been identified as the most appropriate for the project goals, due to its compactness, versatility to incorporate many parameters of concern, and scalability to any circuit size. Based on the selected data structure, a first version of an i-RISC tool for computing the reliability of a circuit was implemented. This tool was further integrated within a Verilog/VHDL Hardware Description Language based design flow, combining custom and academic tools with more established/industry accepted tools, in order to allow evaluation and validation of the project designs at various levels. Moreover, the project has also introduced a Probability Density Functions (PDFs) based Integrated Circuit (IC) reliability assessment framework, which employs a distribution of probabilities for a closer adherence to a faulty circuit stochastic behaviour. The proposed framework, which takes an unorthodox approach towards reliability estimation, yields a fast and scalable reliability assessment approach, to be integrated in reliability aware synthesis tools.

Finally, the project has also started investigations related to the systematic synthesis of fault tolerant combinational circuits, though the concept of error correction driven graph augmentation. A number of circuit classes were identified and a first analysis into the encoding of such circuits was performed.

3.1.4 Main outcomes

The project outcome during this period includes many publications in international conferences and journals, the organisation of high visibility scientific workshops, and a number of contributions to various workshops, special sessions, schools, and working groups, in order to exploit synergies and identify opportunities for co-operation with researchers and projects working in related areas.

Publications. i-RISC partners were very active to ensure a high visibility of the project in prestigious scientific venues. In particular, the project outcome comprises a total of 4 submitted contributions to journals (1 accepted), 12 to conferences (8 accepted), and 10 to workshops.

Workshops organisation. The organisation of workshops is essential to disseminate the project results within the industry and scientific communities. So far, the project has organised one scientific workshop collocated with the European Solid-State Circuits Conference (ESSCIRC), September 2013. The Workshop provided an interaction forum for information and coding theory, circuits and systems, computer engineering, and communication systems researchers, whose research goals aim to advance knowledge and understanding of reliable computing systems built from unreliable components.

Other dissemination activities. In order to exploit synergies and identify opportunities for co-operation with researchers and projects working in related areas, i-RISC partners have also participated in a number of workshops, special sessions, schools, and working groups, providing interaction forums for researchers working in related areas (e.g., GdR-ISIS workshop on error correcting codes for reliable processing with unreliable circuits, FETCH Winter School on design technologies for heterogeneous embedded systems, ITA special session on variability-aware information processing, etc.).

Moreover, a number of communication and awareness raising activities have been initiated, by using well-established links of i-RISC partners with IC companies and knowledge-transfer sector (e.g. MIDAS, MCCI, Qualcomm, Analog Devices, Synopsys, and Hittite Semiconductors).

3.1.5 Expected final results and their potential impact and use

The i-RISC project acts as a pathfinder, which in the long term may lead to completely new and revolutionary solutions for the next-generation low-power electronic circuit design, through the reliable nanoscale integration of chips built out of unreliable components. By the end of the project, we intend to evaluate the potential implications of the proposed approach in real-life scenarios. To this end, proofs of concept are envisaged for key i-RISC approach items and to demonstrate how specific results can be integrated such that a reliable processor can be constructed out of unreliable components.

We believe that the successful demonstration of i-RISC's goal of applying concepts of modern coding theory to the development of novel fault-tolerant devices will provide a new measure of performance in memory and computing systems. Although the primary targeted technology is CMOS, the proposed techniques may be adapted and applied to post-CMOS technologies. In addition to the technical merit of improved system performance, it will also serve as a framework for research in these fields.

The expected technological impact of the i-RISC project can greatly influence the design optimization and the energy efficiency of future electronic circuits, contributing significantly to the evolution of the ICT infrastructure in the Europe and abroad. New coding techniques can improve the performance of memory and computing systems without requiring major improvements in (the physical reliability of) materials and devices. This is especially important at this point in time when the physical properties of the nano devices are being pushed to their limits. The i-RISC project is seen by the consortium's members as one of the most viable paths to continue the life of Moore's law. On a broader scale the results of this work will have a direct impact on the performance capabilities of new generation of memories, computers, and electronic devices, thus benefiting to the society as a whole.

3.1.6 Website and contact details

The project has created a web site (http://www.i-risc.eu/), providing all relevant information on i-RISC, including list of partners and contact details, public deliverables, list of external publications and announcement of events (workshops).

Contact details

Dr. Valentin Savin, project coordinator (valentin.savin@cea.fr)	Commissariat à l'Energie Atomique et aux Energies Alternatives, France.
Prof. David Declercq (declercq@ensea.fr)	Ecole Nationale Supérieure de l'Electronique et de ses Applications, France.
Dr. Sorin Cotofana (S.D.Cotofana@tudelft.nl)	Technische Universiteit Delft, The Netherlands.
Dr. Alexandru Amaricai (amaricai@cs.upt.ro)	Universitatea Politehnica Timisoara, Romania.
Dr. Emanuel Popovici (E.Popovici@ucc.ie)	University College Cork, National University of Ireland.
Dr. Goran Djordjevic (goran.t.djordjevic@elfak.ni.ac.rs) **Prof. Bane Vasic** (vasic@ece.arizona.edu)	University of Nis, Faculty of Electronic Engineering, Serbia.