Analysis of Transient Error Propagation in Sub-Powered CMOS Circuits

S. Nimara, A. Amaricai and M. Popa

***Abstract*—**The quest for lower power consumption has led to aggressive supply voltage scaling till near-threshold and sub-threshold regimes. Reliability represents one of the major concerns in these very low voltage conditions. This paper aims to study the occurrence and propagation of transient errors in noise-affected near and sub-threshold CMOS devices. We have performed SPICE simulation campaigns for 65 nm and 45 nm CMOS circuits operating at very low supply voltages. We have analyzed the impact of the amplitude and duration of pulses corresponding to the transient errors. Although the noise margins of the circuits are diminishing as the supply voltage is lowered, we noticed that transient error propagation is significantly hindered with the decrease in Vdd.

Keywords — near-threshold computing, sub-threshold computing, single-event errors

I. Introduction

Today's nanoscale devices are characterized by high leakage currents, which lead to increased static power (which becomes the dominant factor) and overall power consumption. A promising alternative for future very low power devices is represented by aggressive voltage scaling towards near and sub-threshold Vdd [5]. This strategy targets both the reduction of the static and dynamic components of the power. However, the dramatic decrease in supply voltage will result in both reduced circuit reliability and performance. Regarding the reliability, the problems associated to the very low supply voltages are further augmented by the transistor down-scaling. In these low voltage operating regimes, conventional CMOS circuits are expected to have a probabilistic behavior [7]. Two sources of probabilistic faults exist for sub-powered circuits: transient errors (glitches), due to thermal noise, electromagnetic interference, radiation, etc; the inability of a logic gate to switch in a given amount of time, due to undefined delay characteristics associated with process and voltage variations [1].

The purpose of this paper is represented by the analysis of the transient errors (such as single event upsets (SEUs)) behavior in sub-powered CMOS circuits. On one hand, we examine the effect of the noise amplitude on the behavior of CMOS logic devices in a probabilistic manner. On the other hand, we investigate the relation between the noise pulse width and error propagation in a sub-powered CMOS gate net-list. In both cases, we have performed SPICE simulation using the 65 and 45 nm PTM transistor models for low supply voltages.

The rest of this paper is organized as follows: in Section II we bring into discussion the concept of transient faults, their types and their causes, Section III describes the proposed methodology for analyzing the occurrence and propagation of errors, while Section IV provides the concluding remarks.

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II. Transient Errors

Faults experienced by semiconductor devices can be classified into three main categories: permanent, intermittent and transient. Permanent faults are irreversible and are usually caused by manufacturing defects or device wear-out. Intermittent faults appear because of unstable or marginal hardware and they usually precede the occurrence of permanent faults. Additionally, they occur repeatedly at the same location [3].

Cosmic rays, capacitive coupling, electromagnetic interference, power transients, crosstalk, ground bounce, IR drop or radiation represent the main causes of transient faults [7], [10]. According to [10], a transient fault resulting from a single particle hit is called a single-event transient (SET), while an error in a memory element that was caused either by a SET or from direct radiation hit is referred to as a soft error or a single-event upset. Soft errors occur when highly energetic particles, like protons, neutrons, alpha particles or other heavy ions strike sensitive regions of the silicon [3], [5]. According to [1], such errors are caused by three main radiation mechanisms: alpha particles emitted by trace uranium and thorium impurities in packaging materials, high-energy neutrons from cosmic radiation and low-energy cosmic neutron interactions with the isotope boron-10.

Marculescu and Zivanov discussed in [10] the range of glitch sizes that must be considered when dealing with transient faults that are induced by a specific event, for the 130 nm technology. For that specific technology the duration of glitches pulse duration is situated between 30 and 300 ps, with most glitches having values between 100 and 250 ps.

Regarding the propagation of such glitches, three masking factors have a significant effect [11]:

1. Logical masking – the glitch manifests at the input of a gate when the other inputs have a controlling value (i.e. a "1" glitch arrives at an AND gate input, while the other input is "0").
2. Electrical masking – the glitch is not large enough with respect to gate delay in order to ensure its propagation
3. Latching-window masking – the glitch arrives too late to the input of a latch to be stored;

In this paper, we investigate mostly the electrical masking effect in the sub-powered CMOS circuits.

III. Transient Error Analysis

A. Influence of Noise Amplitude

In order to investigate the influence of the noise amplitude in the overall circuit reliability, we have simulated a simple CMOS circuit consisting of two Inverter gates (Fig. 1). The noise has been applied between the two logic gates. The employed transistor models are represented by the 65 nm PTM models. LT SPICE simulator has been employed for our simulations [9], [10].

In order to analyze the effect of the amplitude of the transient noise, we have employed Monte Carlo simulations consisting of 50.000 individual simulations. We have applied variations on the amplitude of the noise signal. The supply voltages have been varied from 0.8 V to 0.3 V. Therefore, we have covered both the near and the sub-threshold regimes. For each supply voltage, we have used two different Gaussian distributions for the noise signal: one with sigma 0.2 and one with sigma 0.3. We have considered an erroneous result when the gate output crosses the Vdd/2 threshold.

The results are plotted in Fig. 2. We observe that lowering the supply voltage result in a dramatic decrease in the overall gate reliability. Thus, for very low supply voltage, minor noise may result in an erroneous logic output. This represents an expected result as decreasing the supply voltage will result in the decrease of logic gate noise margin, which will make the circuit more prone to transient errors.

B. Influence of Noise Pulse Width

The second set of experiments has consisted in determining the noise pulse width for which the noise will propagate through a logic gate. These have been performed using the 45 nm PTM low power model. We have performed analysis on a two Inverter chain and two 2-input NAND gates chain. The supply voltages have been varied from 0.7 V to 0.2 V, thus covering both sub and near threshold regimes. In these circuits, we have varied the PMOS transistor width with respect to the NMOS transistor width. For the inverter, the considered PMOS had the width equal, double or four times greater than the width of the NMOS transistor (equal to 500 nm).

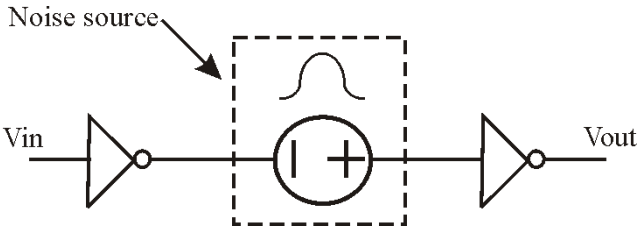

Figure 1. The error modeling circuit

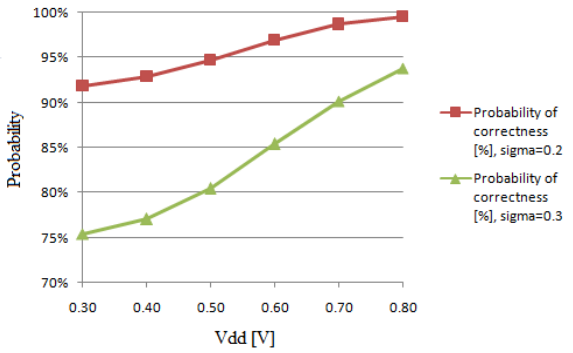

Figure 2. The dependence between Vdd and the probability of correctness

For the NAND gate, the width of the PMOS has been considered half, equal or double with respect to the width of the NMOS transistors (equal to 1000 nm). Both "0" and "1" glitches have been applied. For our analysis, we have not considered the effect of the connecting wires between the gates (given by the resistance and the capacitance of the wire).

Results are presented in Table I-III (for the inverter chain) and IV-VI for the NAND gate chains. They show that "0" glitch propagation is favored when the PMOS drive strength is greater with respect to the NMOS drive strength. Similar, the "1" glitch propagation is favored when the NMOS drive strength is greater.

Regarding the minimum pulse width which ensures propagation, we observe an exponential increase with the down-scaling of the supply voltages. We observe that for 0.7, almost all usual glitches (the ones with width between 100 ps and 300 ps [11]) propagate through one or two gates. However, for sub-threshold voltages, the glitches must have very large duration (several ns and even us) in order to ensure their propagation through even one gate. This electrical masking effect, which is present in low supply voltage regimes, may be augmented by the capacitance and resistance of the interconnecting wires between logic gates.

IV. Conclusions

In this paper, we have analyzed the effects of the pulse width and amplitude typical to transient errors in the CMOS circuits operating at very low supply voltage. Regarding the amplitude, the performed simulations lowering the supply voltage will lead to lower reliability, due to the decreased noise

margins specific for sub-threshold and near-threshold regimes of operations. Regarding the propagation of transient faults, devices operating at lower Vdd show increased resilience to these types of faults. The simulation results show that glitches with narrower pulses propagate better for higher supply voltages. The electrical masking effects in sub-powered CMOS circuits represent an important factor which limits error propagation through a logic circuit. In real circuits, the electrical masking is also amplified by the interconnecting wires between logic gates.

This paper shows that the effect of glitches generated by thermal noise, radiation, electromagnetic interference, have a limited impact in the overall reliability of circuits operating at sub and near threshold voltages.

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TABLE I – MINIMUM PULSE WIDTH WHICH ENSURES GLITCH PROPAGATION THROUGH TWO INVERTERS

$(width_{PMOS} = width_{NMOS})$

Vdd [V]	Minimum pulse width[ns] "0" Glitch		Minimum pulse width[ns] "1" Glitch	
	Gate 1	Gate 2	Gate 1	Gate 2
0.2	630	1530	390	1040
0.3	57	156	36	103
0.4	5.25	15.7	3.4	10.1
0.5	0.6	1.85	0.35	1.26
0.6	0.1	0.3	0.06	0.19
0.7	0.03	0.09	0.02	0.05

TABLE II – MINIMUM PULSE WIDTH WHICH ENSURES GLITCH PROPAGATION THROUGH TWO INVERTERS

$(width_{PMOS} = 2 * width_{NMOS})$

Vdd [V]	Minimum pulse width[ns] "0" Glitch		Minimum pulse width[ns] "1" Glitch	
	Gate 1	Gate 2	Gate 1	Gate 2
0.2	480	1290	610	1480
0.3	43	128	56	150
0.4	4	12.7	5.2	14.9
0.5	0.45	1.49	0.6	1.75
0.6	0.08	0.24	0.1	0.28
0.7	0.03	0.07	0.03	0.08

TABLE III – MINIMUM PULSE WIDTH WHICH ENSURES GLITCH PROPAGATION THROUGH TWO INVERTERS

$(width_{PMOS} = 4 * width_{NMOS})$

Vdd [V]	Minimum pulse width[ns] "0" Glitch		Minimum pulse width[ns] "1" Glitch	
	Gate 1	Gate 2	Gate 1	Gate 2
0.2	410	1205	1050	2290
0.3	37	116	95	240
0.4	3.4	11.3	8.8	24.1
0.5	0.38	1.32	1	2.85
0.6	0.06	0.21	0.16	0.46
0.7	0.02	0.07	0.05	0.12

TABLE IV – MINIMUM PULSE WIDTH WHICH ENSURES GLITCH PROPAGATION THROUGH TWO NAND GATES

($width_{PMOS} = 0.5 * width_{NMOS}$)

Vdd [V]	Minimum pulse width[ns] "0" Glitch		Minimum pulse width[ns] "1" Glitch	
	Gate 1	Gate 2	Gate 1	Gate 2
0.2	1110	2390	795	2080
0.3	103	251	82	212
0.4	9.3	25.5	8.2	21
0.5	1.06	3.02	0.97	2.46
0.6	0.17	0.49	0.16	0.4
0.7	0.06	0.15	0.04	0.11

TABLE V – MINIMUM PULSE WIDTH WHICH ENSURES '0' GLITCH PROPAGATION THROUGH TWO NAND GATES

($width_{PMOS} = width_{NMOS}$)

Vdd [V]	Minimum pulse width[ns] "0" Glitch		Minimum pulse width[ns] "1" Glitch	
	Gate 1	Gate 2	Gate 1	Gate 2
0.2	820	1990	1180	2770
0.3	74	204.5	119	291
0.4	6.9	20.7	11.9	29.3
0.5	0.78	2.44	1.4	3.45
0.6	0.13	0.4	0.22	0.57
0.7	0.04	0.12	0.06	0.15

TABLE VI – MINIMUM PULSE WIDTH WHICH ENSURES '0' GLITCH PROPAGATION THROUGH TWO NAND GATES

($width_{PMOS} = 2 * width_{NMOS}$)

Vdd [V]	Minimum pulse width[ns] "0" Glitch		Minimum pulse width[ns] "1" Glitch	
	Gate 1	Gate 2	Gate 1	Gate 2
0.2	670	1895	1930	4080
0.3	61	191	200	441
0.4	5.7	19.3	19.2	45.1
0.5	0.64	2.3	2.25	5.33
0.6	0.1	0.38	0.37	0.87
0.7	0.03	0.11	0.1	0.23