Interconnect Crosstalk Analysis in Sub-powered Integrated Circuits

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Outline

- Motivation & Goal
- Introduction in interconnects
- Interconnect modeling
- SPICE simulations
- Conclusions

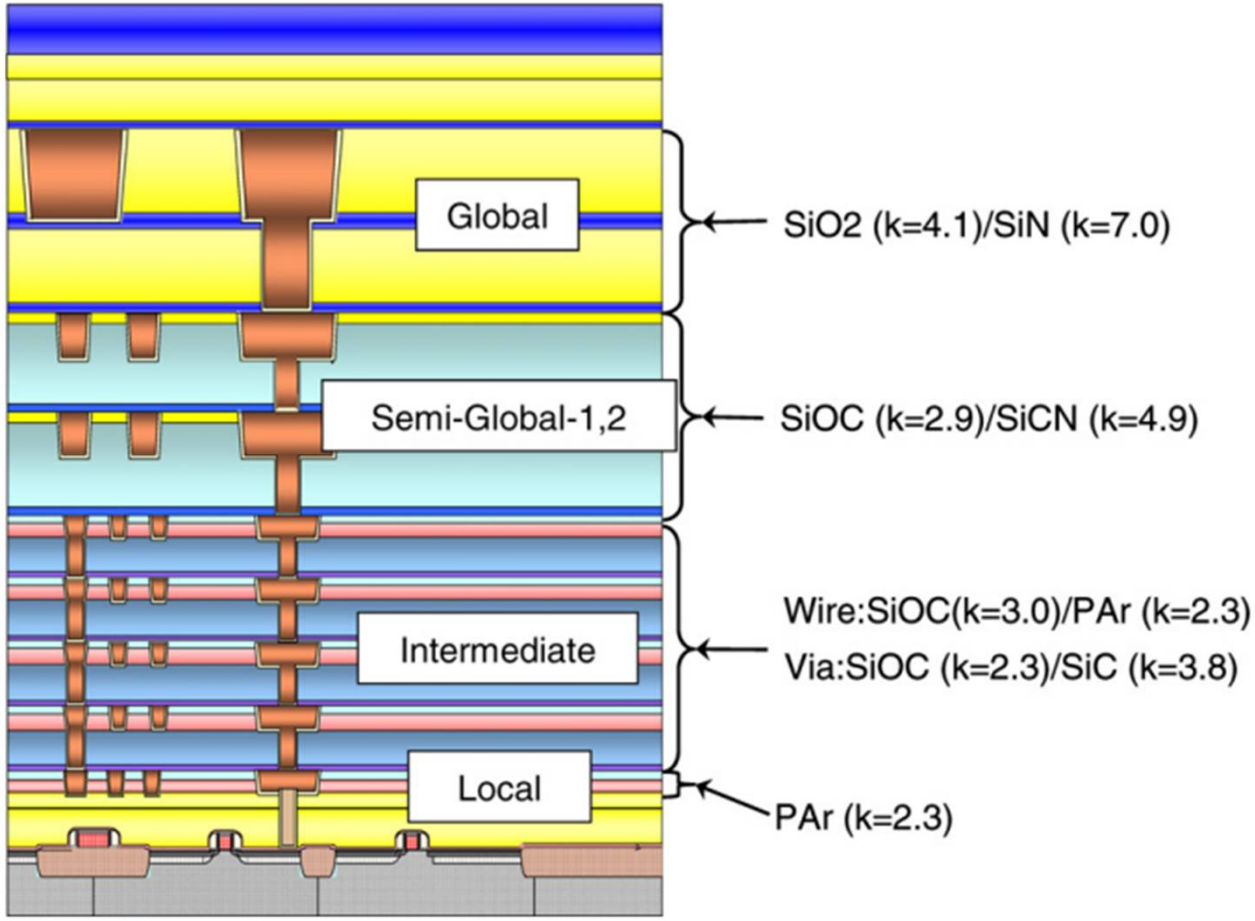
Motivation & Goals

- Determine data dependence error models for interconnects
  - Logic level alteration
  - Delay dependent error models
- Establish design guidelines for interconnects
  - Determine wire spacing & length
  - Parameters:
    - Supply voltage (range)
    - Dielectric material
    - Maximum number of accepted errors

Goals

- Determine the minimum spacing
  - Larger spacing -> greater cost
  - Increase number of wires on plane
  - Very large transports
- Determine the maximum length
  - Reduction of repeater buffers for long interconnects
    - Reduction of silicon usage
    - Reduction of metallic vias

Introduction in interconnect



45/32 nm CMOS – Challenge and perspective –
K. Ishimaru, Solid State Electronics, 2008

$$R = \frac{\rho \cdot l}{w \cdot t}$$

Interconnect electrical properties

- Resistance
  - Depends on physical characteristics
  - Timing parameters of a wire
  - Power consumption characteristics of a wire

$$R = \rho * \frac{l}{S}$$

- Inductance
  - Self inductance
    - Depends on the length & perimeter
    - Voltage increase/decrease when switching

$$L_s = \mu_0 * \frac{l}{2\Pi}\left[\ln\left(2l/p\right) + 1/2 + 0.22 * p/l\right]$$

*ptm.asu.edu

Interconnect electrical properties

- Inductance
  - Mutual inductance
    - Inductive cross-coupling
    - Wide range affect (spans multi-wires)
    - Depends on the wire spacing and length

$$M = \mu_0 * \frac{l}{2\Pi}\left[\ln\left(2l/d\right) - 1 + d/l\right]$$

- Capacitance
  - Ground capacitance
    - Depends on wire spacing & dielectric material

$$C_g = \varepsilon\left[w/h + 2.04 * \left(s/s + 0.54 * h\right)^{1.77}\right]$$

  - Cross-coupled capacitance
    - Neighbor wires affected

$$C_c = \varepsilon\left[1.41 * t/s * e^{-\frac{4s}{s+8.01h}} + 2.37 * \left(w/w + 0.31s\right)^{0.28} * \left(h/h + 8.91s\right)^{0.76} * e^{-\frac{2s}{s+6h}}\right]$$

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Noise sources in interconnects

- Crosstalk
  - Inductance/Capacitance crosstalk
  - Substrate crosstalk
    - Passive components in substrate
  - Power/ground line crosstalk
- Transmission line effects
  - Affects long lines (global)
  - Depends on the signal frequency
  - Due to impedance discontinuities
    - Vias, wire bends, cross-over lines, etc
    - Process defects (bubbles, diffusion, etc)
- Electro-magnetic interference

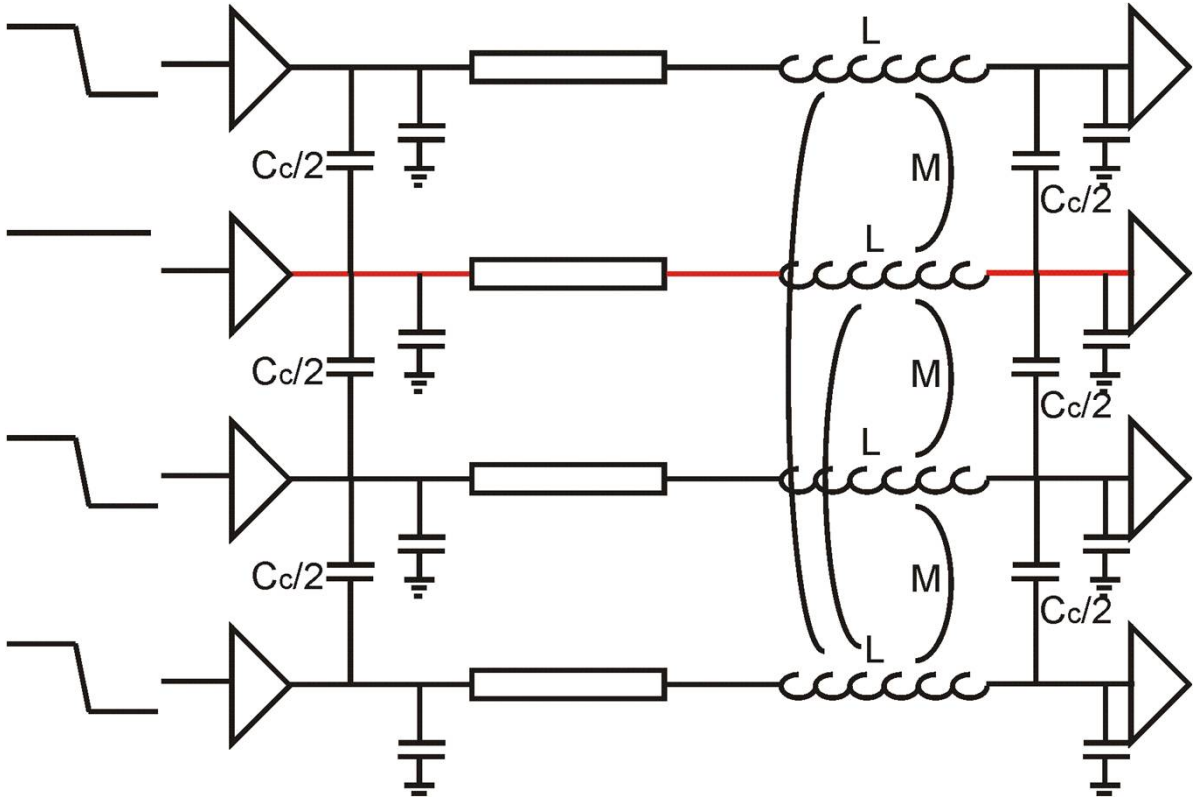
Interconnect modeling

- RC models
  - Inductors' influence is around 5%
  - Pi model of the wire
- RLC models
  - Include inductors
  - Second degree differential equations
- RLCG models
  - Include very large resistor between wires
  - Conductance through the dielectric material.

Simulation scenario

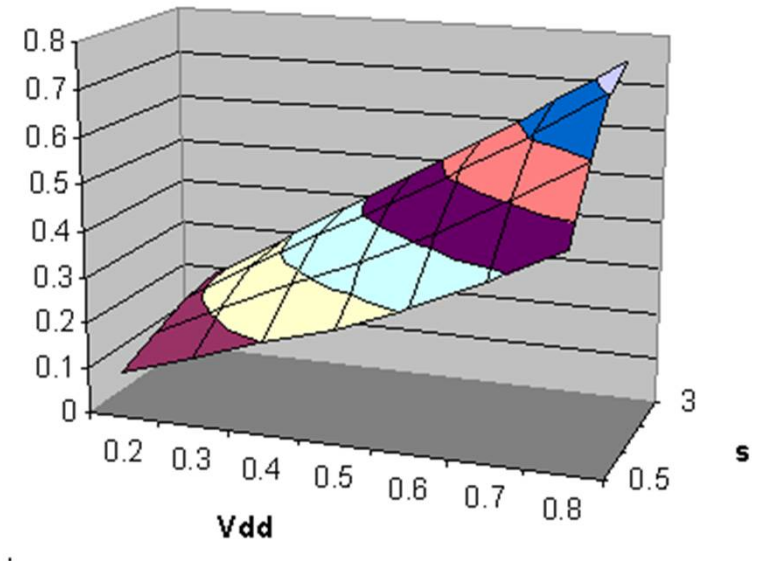
- 4-wire interconnect RLC model
- 4 driver buffers & 4 receiver buffers
- Victim line – internal wire
- 560 simulations
- Parameters:
  - Spacing
  - Length
  - Dielectric constant
  - Vdd

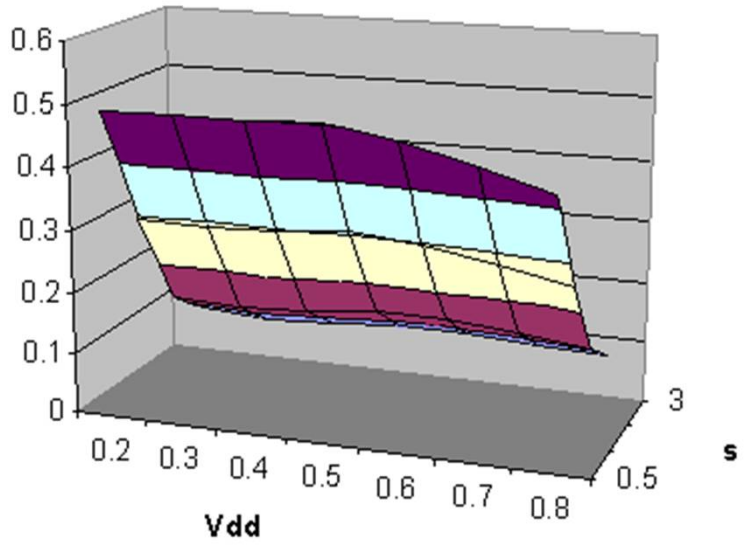
Simulation scenario



Simulation results
Dependence on spacing

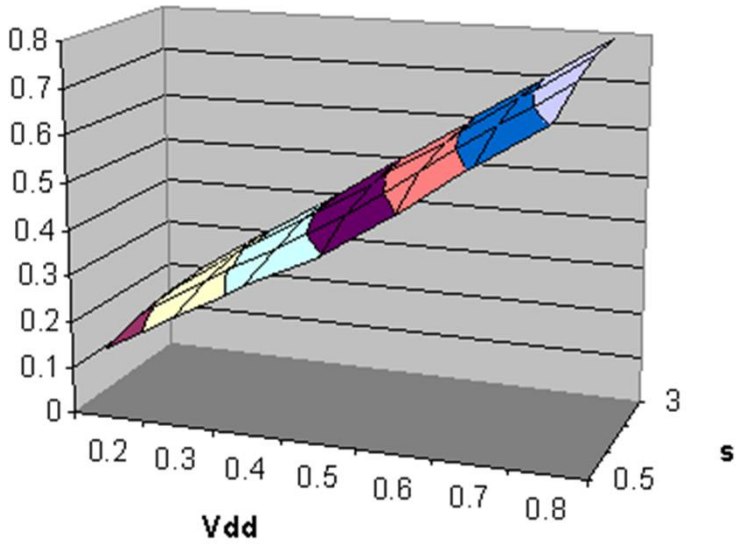
- L=100 um k = 3

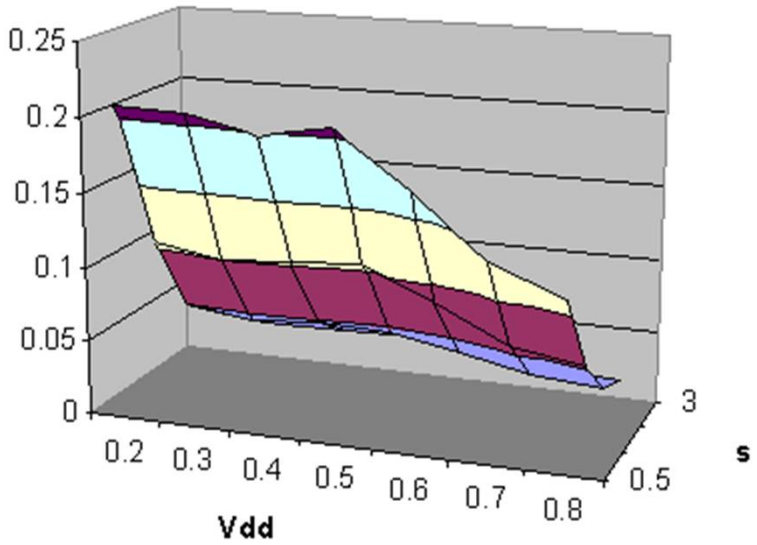




Simulation results
Dependence on spacing

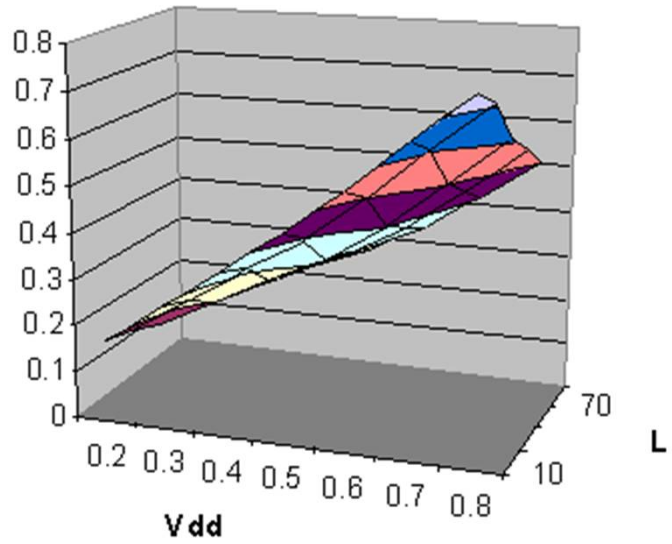
- L = 20 um k = 2.2

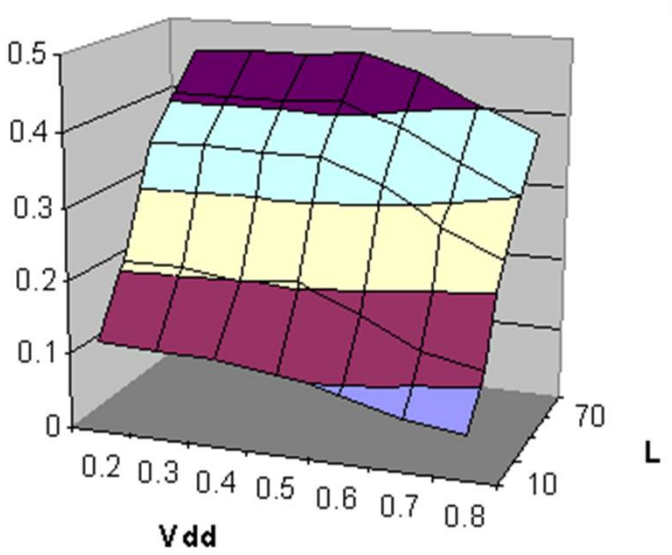




Simulation results
Dependence on length

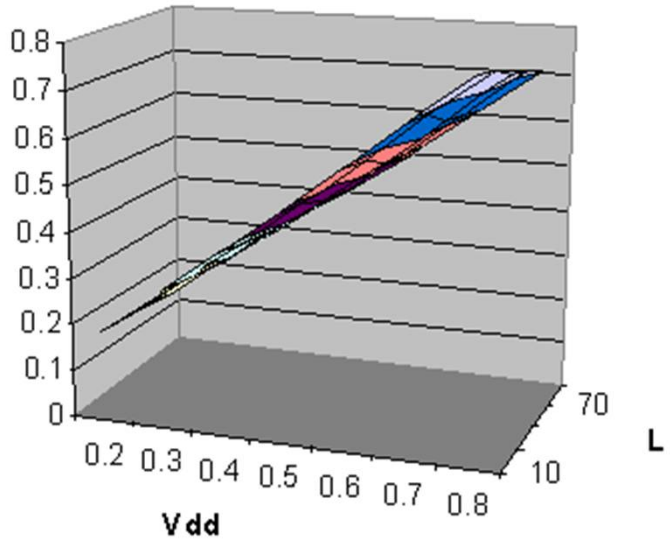
- k = 2.2 s = 0.5

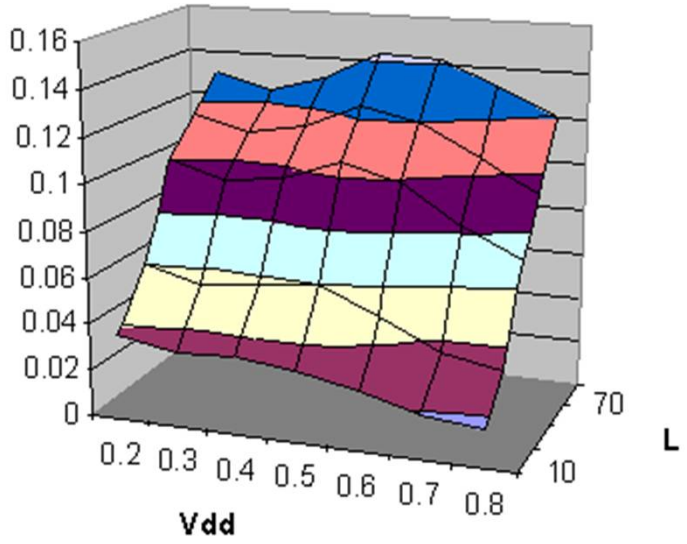




Simulation results
Dependence on length

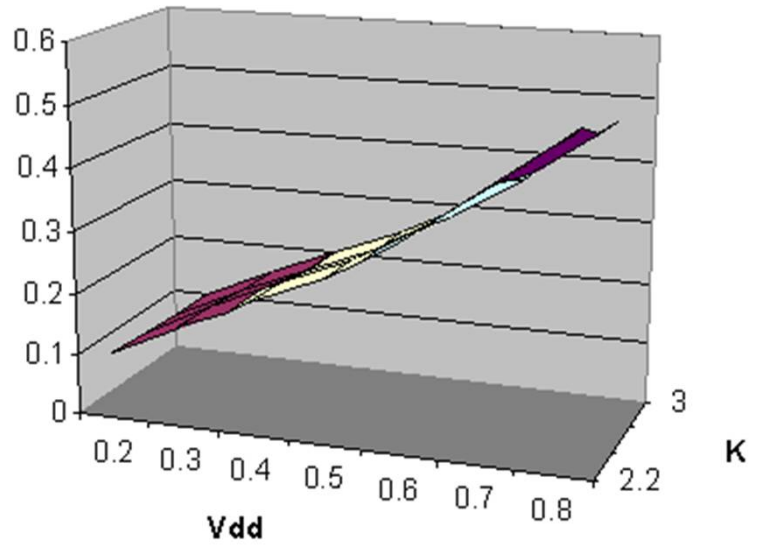
- k = 3 s = 2

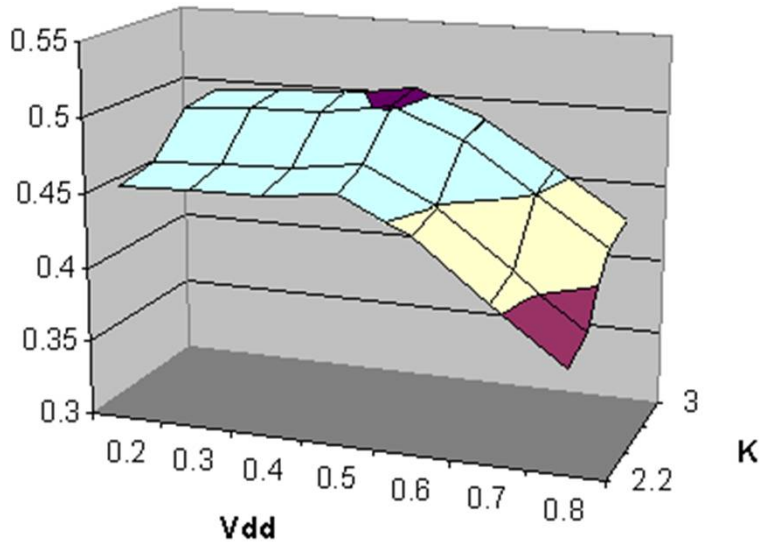




Simulation results
Dependence on dielectric constant

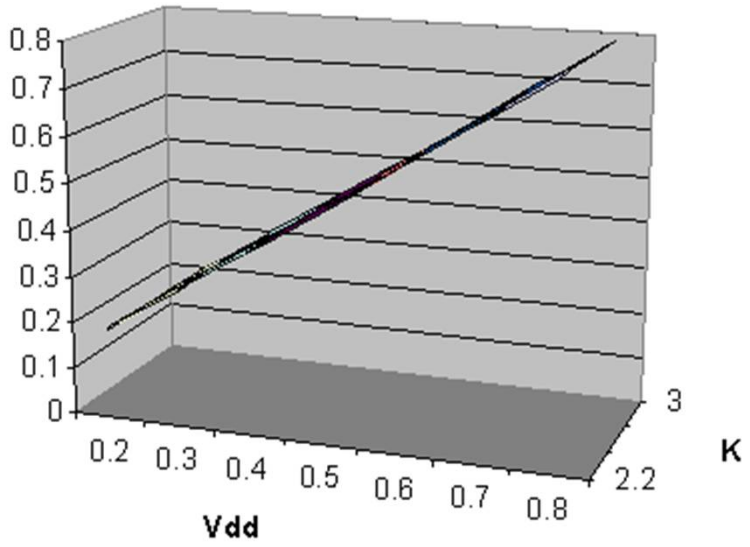
L= 100 um s = 0.5 um

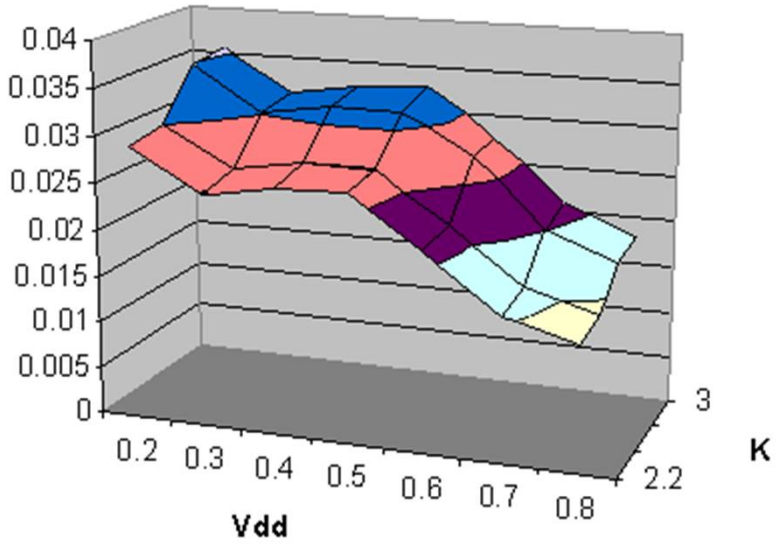




Simulation results
Dependence on dielectric constant

- L=20 um s = 3 um





Conclusions

- Investigate the crosstalk effects in low supply voltage regions of operations
- Investigate the influence of different parameters (length, spacing, dielectric material)
- Logic level drop – small differences with respect to supply voltage
  - Maximum at around 0.5 V

Thank you